

CIR-W5SUSB4832G

DDR5 WIDE TEMP. SO-DIMM 4800MHz 32GB

Description

CIR-W5SUSB4832G is a 4G x 64-bit (32GB) DDR5-4800 CL40 SDRAM (Synchronous DRAM), 2Rx8, memory module, based on eight 2G x 8-bit FBGA components. The SPD is programmed to JEDEC standard latency DDR5-4800 timing of 40-39-39 at 1.1V. Each 262-pin SO-DIMM uses gold contact fingers. Power management integrated circuit (PMIC) provides better signal integrity and more stable power. Original DRAM chips and all components are stringently tested for the highest level of compatibility, reliability, and performance.

Specifications

| | |
|------------------------|-------------------|
| Density | 32GB |
| Pin Count | 262pin |
| Type | Unbuffered |
| Dimensions | 69.60mm x 30.00mm |
| ECC | Non-ECC |
| Component Config | 2G x 8 bit |
| Data Rate | 4800 MHz |
| CAS Latency | 40 |
| Voltage | 1.1V |
| PCB Layers | 10 |
| Operating Temp.(TCASE) | -40°C~+85°C |
| Module Ranks | Dual Rank |

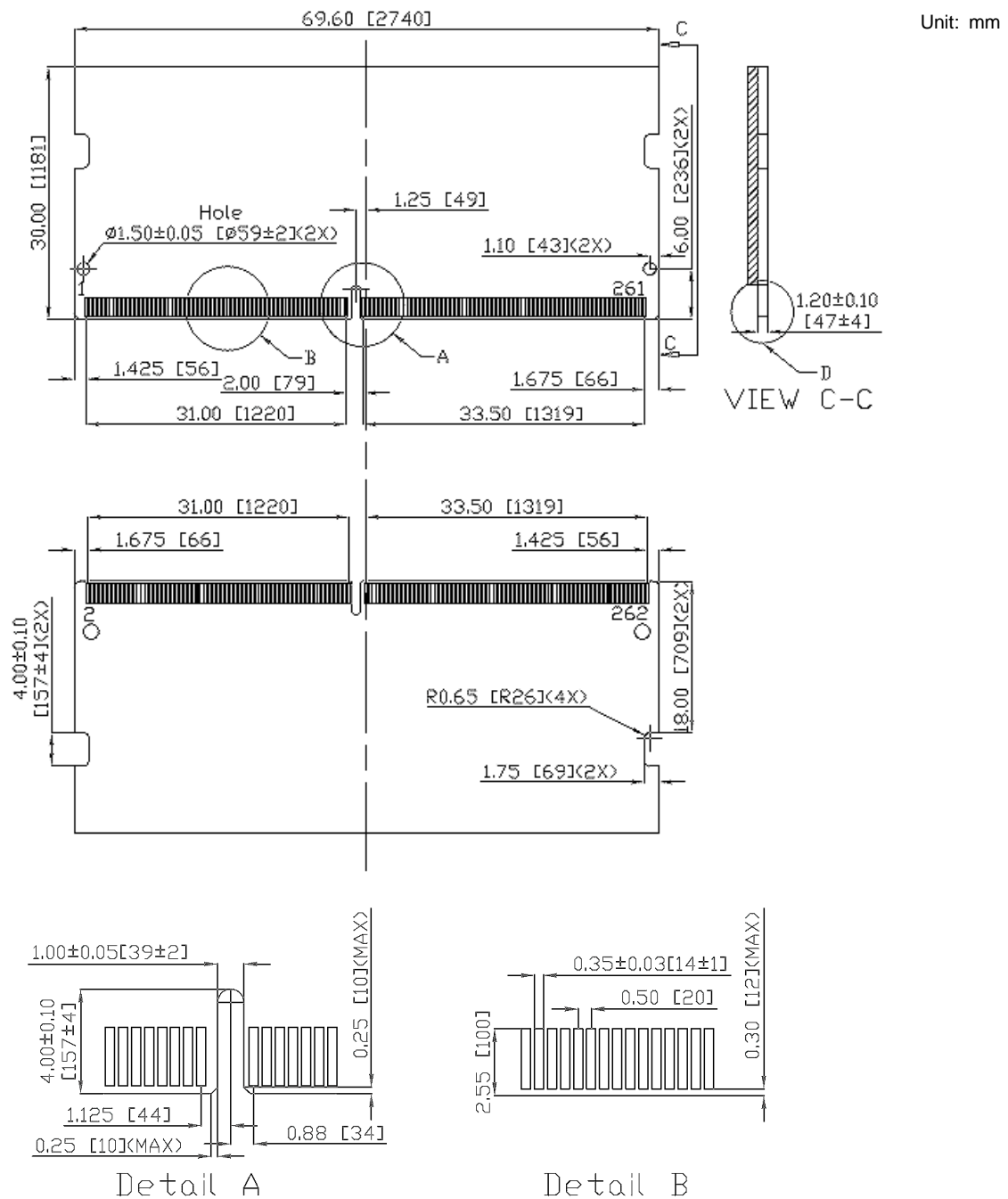
Features

- JEDEC Standard 262-pin Small Outline Dual In-Line Memory Module
- VDD = VDDQ = 1.1V (1.067V~1.166V)
- VPP = VDDSPD =1.8V
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42
- PMIC on DIMM, nominal supply 5V, VIN_Bulk input supply range: 4.25 V to 5.5 V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- On-Die ECC
- SPD Hub with Thermal Sensor
- Fly-By topology
- Terminated control, command and address bus
- RoHS Compliant and Halogen free

Speed Grade

| Frequency Grade | Data Transfer Rate | CAS Latency Support | | | CL-tRCD-tRP |
|-----------------|--------------------|---------------------|-----|-----|-------------|
| | | CL40 | TBD | TBD | |
| DDR5-4800 | PC5-38400 | 4800 | TBD | TBD | 40-39-39 |

Package Dimensions



Tolerances: ± 0.15 mm unless otherwise specified