



MODEL:
DRPC-W-TGL Series

Fanless System with Intel® Tiger Lake-U Processors, Triple 2.5GbE LAN, HDMI, DP, 8GB Memory Pre-installed, 12V DC and RoHS

User Manual

Revision

| Date | Version | Changes |
|------------------|---------|-----------------|
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Manual Conventions



WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.



CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.



NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.



HOT SURFACE

This symbol indicates a hot surface that should not be touched without taking care.

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Chapter

1

Introduction

1.1 Overview



Figure 1-1: DRPC-W-TGL Series

The DRPC-W-TGL Series is an embedded system for wide range temperature environments. It is powered by Intel® Tiger Lake-U processor, and pre-installed 8GB DDR4 SO-DIMM memory (up to 32GB). The DRPC-W-TGL Series includes two HDMI, one DP, three 2.5GbE LAN ports, four USB 3.2 Gen2 ports, and one external fan connector.

DRPC-W-TGL

1.2 Feature

The DRPC-W-TGL Series features are listed below:

- Supported CPU:
 - Intel® Core® i7-1185G7E 1.8 GHz (up to 4.4 GHz, quad-core, TDP 15W)
 - Intel® Core® i5-1145G7E 1.5 GHz (up to 4.1 GHz, quad-core, TDP 15W)
 - Intel® Core® i3-1115G4E 2.2 GHz (up to 3.9 GHz, dual-core, TDP 15W)
 - Intel® Celeron® 6305 1.8 GHz (dual-core, TDP 15W)
- Support three independent display
- 3 x 2.5GbE ports
- 1 x M.2 A Key
- 1 x M.2 B Key (with SIM card slot)

1.3 Model Variations

The model variations of the DRPC-W-TGL Series are listed below (Table 1-1).

| Model No. | CPU |
|----------------------|--|
| DRPC-W-TGL-U-CC-R10 | Intel® Celeron™ 6305 1.8GHz (dual core, TDP 15W) |
| DRPC-W-TGL-U-i3C-R10 | Intel® Core™ i3-1115G4E 2.2 GHz (up to 3.9 GHz, dual-core, TDP 15W) |
| DRPC-W-TGL-U-i5C-R10 | Intel® Core™ i5-1145G7E 1.5 GHz (up to 4.1 GHz, quad-core, TDP 15W) |
| DRPC-W-TGL-U-i7C-R10 | Intel® Core™ i7-1185G7E 1.8 GHz (up to 4.4 GHz, quad-core, TDP 15W) |

Table 1-1: DRPC-W-TGL Series Model Variations

1.4 Technical Specifications

The DRPC-W-TGL Series technical specifications are listed in Table 1-2

| Model Name | | DRPC-W-TGL-U-i7C-R10 | DRPC-W-TGL-U-i5C-R10 | DRPC-W-TGL-U-i3C-R10 | DRPC-W-TGL-U-CC-R10 |
|---------------------|------------------------|--|---|---|--|
| Chassis | Color | Black | | | |
| | Dimensions (WxDxH)(mm) | 176x116x67.8 | | | |
| | System Fan | Fanless | | | |
| | Chassis Construction | Extruded aluminum alloys | | | |
| Mother board | CPU | Intel® Core™ i7-1185G7E 1.8GHz (up to 4.4GHz, quad-core, TDP 15W) | Intel® Core™ i5-1145G7E 1.5GHz (up to 4.1GHz, quad-core, TDP 15W) | Intel® Core™ i3-1115G4E 2.2GHz (up to 3.9GHz, dual-core, TDP 15W) | Intel® Celeron™ 6305 1.8GHz (dual-core, TDP 15W) |
| | Chipset | SOC | | | |
| | Memory | 1x DDR4 3200MHz SO-DIMM (pre-installed 8GB) (up to 16GB) | | | |
| Storage | HDD Bay | 1 x 2.5" SATA 6Gb/s HDD bay | | | |
| IO Interfaces | USB | 4 x USB3.2 | | | |
| | LAN | 3 x 2.5GbE | | | |
| | Display | 1 x DP, 2 x HDMI | | | |
| | Others | 1 x Power button, 1 x Reset button, 1 x Power LED, 1 x HDD LED, 1 x System fan connector | | | |
| Internal Expansions | M.2 | 1 x M.2 A Key 2230 for WIFI & BT(optional) 1 x M.2 B Key(PCIe x2) 3042/3052 w/SIM slot for 5G(optional) | | | |
| Power | Power Input | 12V | | | |
| | Power Consumption | 12V@4.1A (Intel i5-1145G7E with 8GB DDR4 Memory) | | | |
| Reliability | Mounting | DIN-Rail | | | |
| | Operating Temperature | -20°C ~ 60°C with airflow, 10% ~ 95% non-condensing | | | |
| | Storage Temperature | -30°C ~ 85°C, 10% ~ 95% non-condensing | | | |
| | Operating Shock | Half-sine wave shock 5G, 11ms, 100 shocks per axis | | | |
| | Operating Vibration | 10-500 Hz, 1.04 Grms, random, 1 hr/axis | | | |
| | Weight (Net/Gross) | 0.98/1.2 KG | | | |
| | Safety/EMC | CE/FCC | | | |
| | Watchdog Timer | Programmable 1 ~ 255 sec/min | | | |
| OS | Supported OS | Microsoft © Windows 10 / Windows 11, Linux | | | |

Table 1-2: Technical Specifications

DRPC-W-TGL

1.5 Front Panel

The front panel of the DRPC-W-TGL Series has the following features.

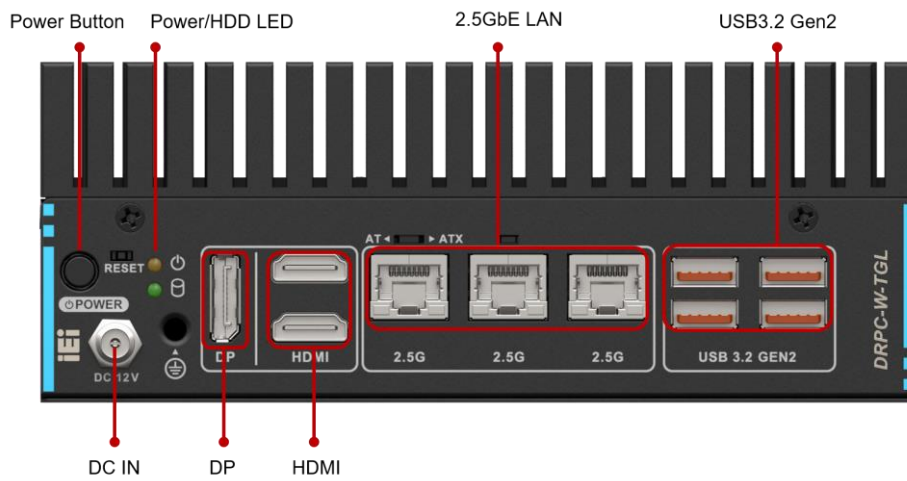


Figure 1-2: Front Panel

1.6 Top Panel

The top panel of the DRPC-W-TGL Series is shown below.

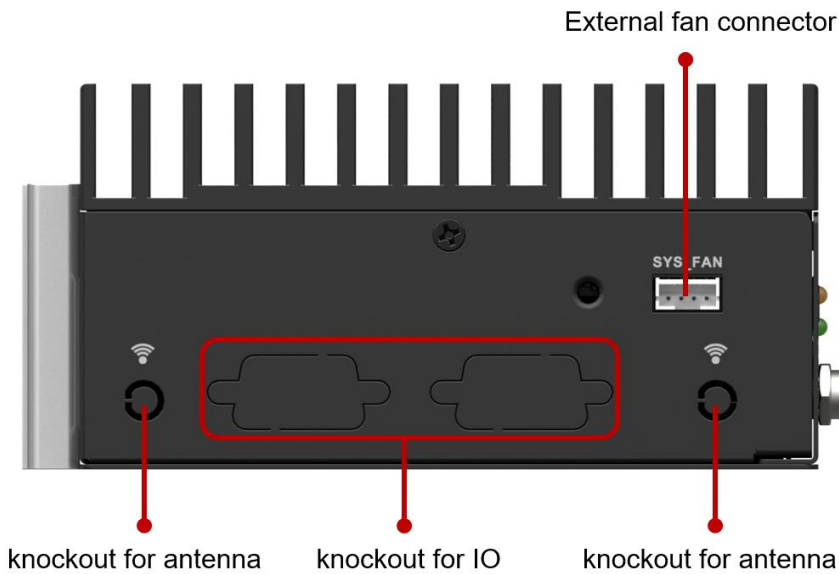


Figure 1-3: Top Panel

1.7 Physical Dimensions

The physical dimensions are shown in Figure 1-4.

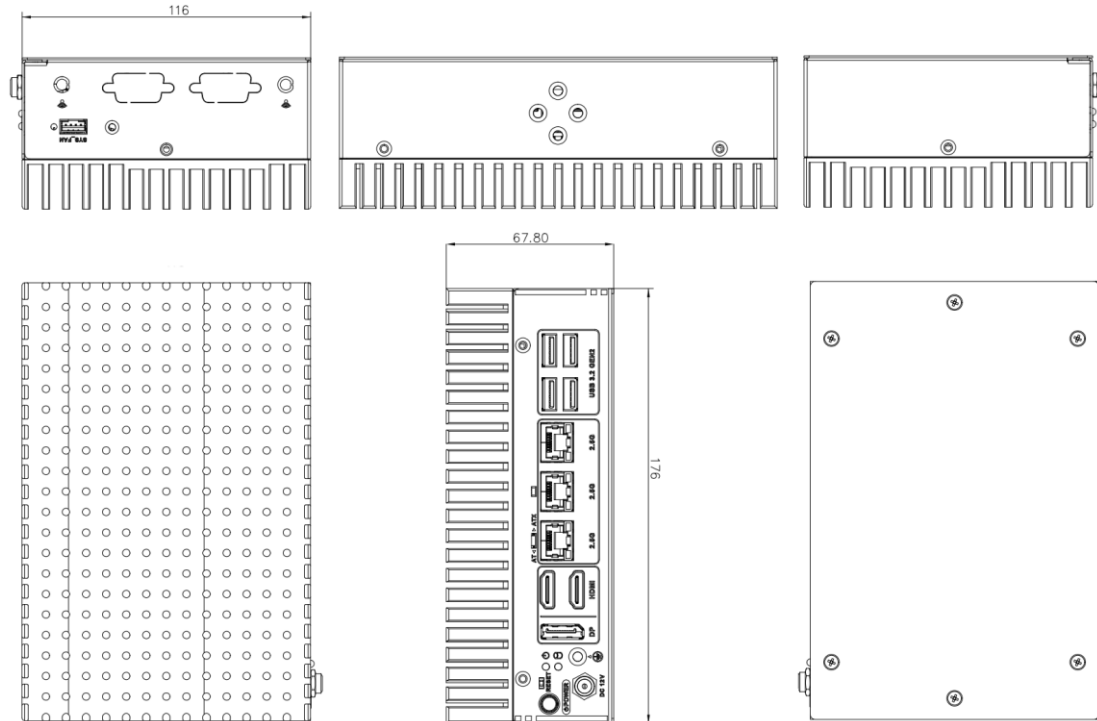


Figure 1-4: Physical Dimensions

Chapter

2

Unpacking

2.1 Anti-static Precautions



WARNING:

Failure to take ESD precautions during installation may result in permanent damage to the DRPC-W-TGL Series and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the DRPC-W-TGL Series. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the DRPC-W-TGL Series or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- **Wear an anti-static wristband:** Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- **Self-grounding:** Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- **Use an anti-static pad:** When configuring the DRPC-W-TGL Series, place it on an anti-static pad. This reduces the possibility of ESD damaging the DRPC-W-TGL Series.

2.2 Unpacking Precautions

When the DRPC-W-TGL Series is unpacked, please do the following:

- Follow the anti-static precautions outlined in **Section 2.1**.
- Make sure the packing box is facing upwards so the DRPC-W-TGL Series does not fall out of the box.
- Make sure all the components shown in **Section 2.2** are present.

DRPC-W-TGL



2.3 Unpacking Checklist




NOTE:

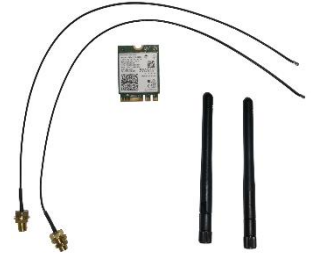


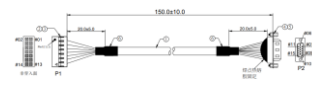

If some of the components listed in the checklist below are missing, please do not proceed with the installation. Contact the IEI reseller or vendor you purchased the DRPC-W-TGL Series from or contact an IEI sales representative directly. To contact an IEI sales representative, please send an email to sales@ieiworld.com.

The DRPC-W-TGL Series is shipped with the following components:


| Quantity | Item and Part Number | Image |
|-----------------|-----------------------|---|
| Standard | | |
| 1 | DRPC-W-TGL Series |  |
| 2 | DIN rail mounting kit |  |

| Quantity | Item and Part Number | Image |
|-----------------|----------------------|---|
| Standard | | |
| 1 | Chassis screws |  |

The following table lists the optional items that can be purchased separately.

| Optional | |
|---|---|
| Wi-Fi module (P/N: EMB-WIFI-KIT02I3-R10) |  |
| VGA module (P/N: iDPM-VGA-R10) |  |
| Serial cable (P/N: 32005-003500-200-RS) |  |
| GPIO cable (P/N: 32031-000600-100-RS) |  |
| Power adapter (P/N: 63040-010060-211-RS) |  |

DRPC-W-TGL

| Optional | |
|--------------------------------------|--|
| Power cord (P/N: 32000-000002-RS) |  |

** Each Wi-Fi module needs two antennas and two RF cables to fully support Wi-Fi function.*

Chapter

3

Installation

DRPC-W-TGL

3.1 Installation Precautions

During installation, be aware of the precautions below:

- **Read the user manual:** The user manual provides a complete description of the DRPC-W-TGL Series, installation instructions and configuration options.
- **DANGER! Disconnect Power:** Power to the DRPC-W-TGL Series must be disconnected during the installation process, or before any attempt is made to access the rear panel. Electric shock and personal injury might occur if the rear panel of the DRPC-W-TGL Series is opened while the power cord is still connected to an electrical outlet.
- **Qualified Personnel:** The DRPC-W-TGL Series must be installed and operated only by trained and qualified personnel. Maintenance, upgrades, or repairs may only be carried out by qualified personnel who are familiar with the associated dangers.
- **Air Circulation:** Make sure there is sufficient air circulation when installing the DRPC-W-TGL Series. The DRPC-W-TGL Series cooling vents must not be obstructed by any objects. Blocking the vents can cause overheating of the DRPC-W-TGL Series. Leave at least 5 cm of clearance around the DRPC-W-TGL Series to prevent overheating.
- **Grounding:** The DRPC-W-TGL Series should be properly grounded. The voltage feeds must not be overloaded. Adjust the cabling and provide external overcharge protection per the electrical values indicated on the label attached to the back of the DRPC-W-TGL Series.

3.2 Cover Removal

Before installing or maintaining the internal components, the cover must be removed from the DRPC-W-TGL Series. Follow the steps below to complete the task.

Step 1: Loosen the 6 screws on the cover.

Step 2: Take off the cover (Figure 3-1).



Figure 3-1: Remove the Cover

3.3 Hard Disk Bracket Removal

Loosen the four screws and remove the hard disk bracket (Figure 3-2).



Figure 3-2: Take out the Disk Bracket

3.4 Storage Installation

The DRPC-W-TGL Series supports two types of storage, one M.2 B Key & one 2.5" SSD

DRPC-W-TGL

3.4.1 2.5-inch SSD Installation

Put the hard disk bracket on the hard disk, secure the bracket with 4 screws, and connect the SATA cable

Install the hard disk and bracket back to the host (Figure 3-3).

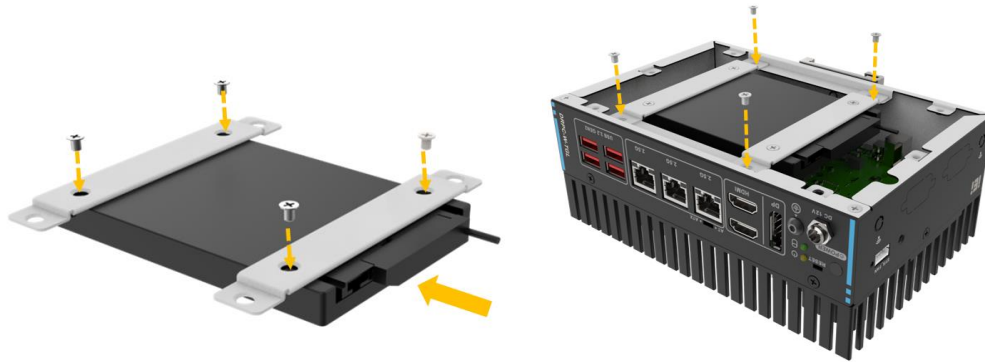


Figure 3-3: HDD Installation

3.4.2 M.2 SSD Installation

To install an M.2 B Key NVME, please follow the steps below.

Step 1: Locate the M.2 module slot.

Step 2: Remove the retention screw secured on the motherboard.

Step 3: Line up the notch on the module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20° (Figure 3-4).

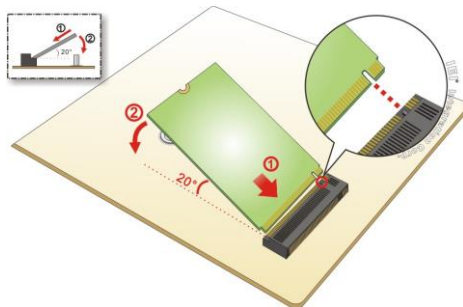


Figure 3-4: Inserting the M.2 Module into the Slot at an Angle

Step 4: Secure the M.2 module with the previously removed retention screw (Figure 3-5).

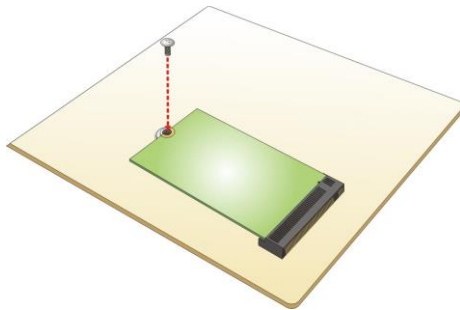


Figure 3-5: Securing the M.2 Module

3.5 Wi-Fi Module Installation (Optional)

The Wi-Fi module is an optional accessory. You can purchase it from IEI or other providers. Note that you have to purchase Wi-Fi module, internal antenna and external antenna. It is suggested to purchase an internal antenna longer than 200mm.

To install the Wi-Fi module, follow the steps below.

Step 1: Locate the M.2 A Key module slot.

Step 2: Remove the retention screw secured on the motherboard.

Step 3: Line up the notch on the WLAN module with the notch on the slot. Slide the WLAN module into the slot at an angle of about 20° (Figure 3-6).

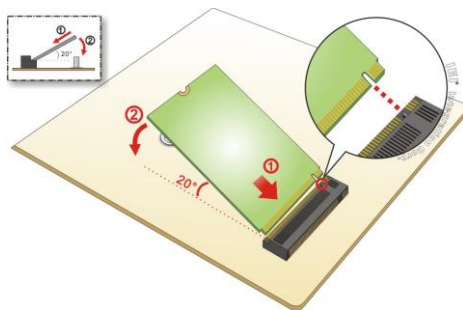


Figure 3-6: Inserting the WLAN Module

Step 4: Secure the WLAN module with the retention screw previously removed (Figure 3-7).

DRPC-W-TGL

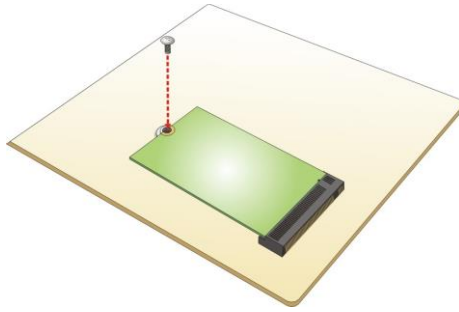


Figure 3-7: Securing the WLAN Module

Step 5: Connect the two RF cables to the antenna connectors on the WLAN module (Figure 3-8).

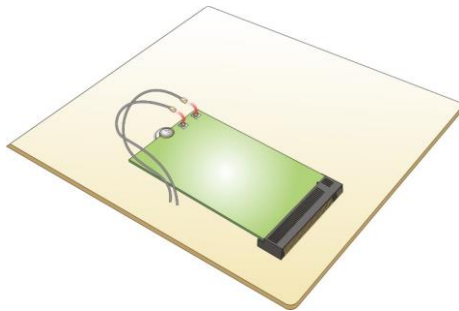


Figure 3-8: Connecting RF Cables

Step 6: Remove the nut and washer from the SMA connector at the other end of the RF cable.

Step 7: Knock out the reserved antenna holes on the chassis. Insert the SMA connector to the antenna connector holes on the rear panel.

Step 8: Secure the SMA connector by inserting the washer and tightening it with nut.

Step 9: Install the external antenna (Figure 3-9).

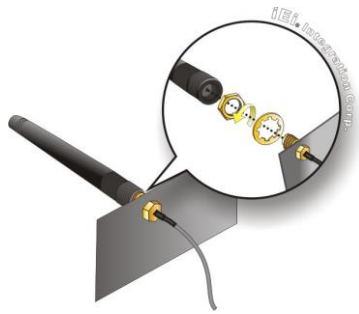


Figure 3-9: Securing SMA Connector and External Antenna Installation

3.6 Expansion I/O Installation (Optional)

The DRPC-W-TGL Series has reserved GPIO port, serial port, iDPM slot for function expansions. Optional cable or module are ready for purchase. To install these expansion components, follow the steps below.

3.6.1 Serial Port Installation

Step 1: Locate the Serial port connector.

Step 2: Connect the serial cable to the serial connector on the mainboard.



Figure 3-10: Connect the serial cable to the serial connector

Step 3: Knock out the reserved holes on the chassis and Secure the DB9 end of the serial cable to the panel.

DRPC-W-TGL

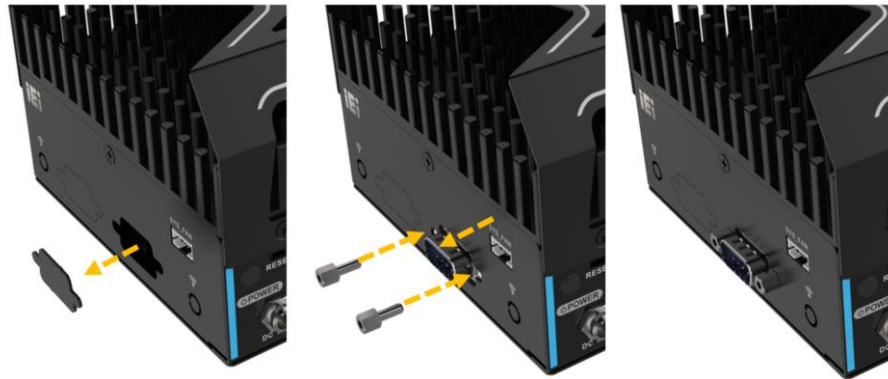


Figure 3-11: Knock out the reserved holes

3.6.2 GPIO Installation

Step 1: Locate the GPIO port connector.

Step 2: Connect the GPIO cable to the GPIO connector on the mainboard.

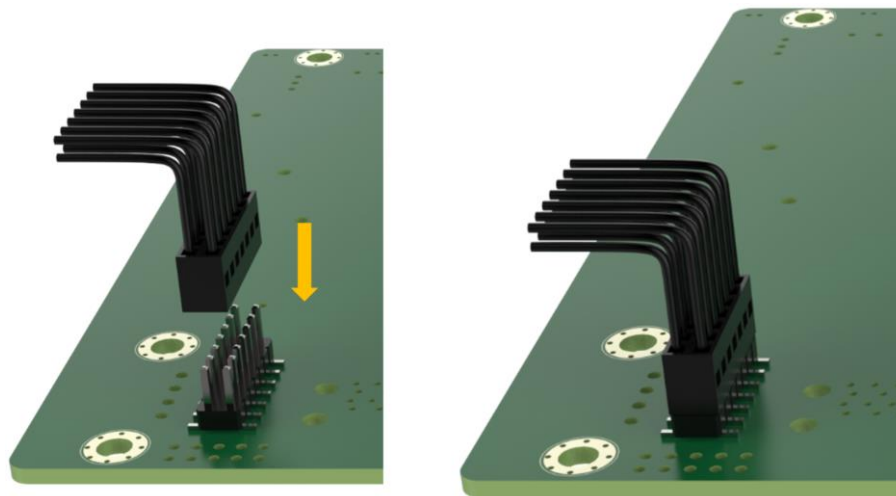


Figure 3-12: Connect the GPIO cable to the GPIO connector

Step 3: Knock out the reserved holes on the chassis and Secure the DB15 end of the GPIO cable to the panel.

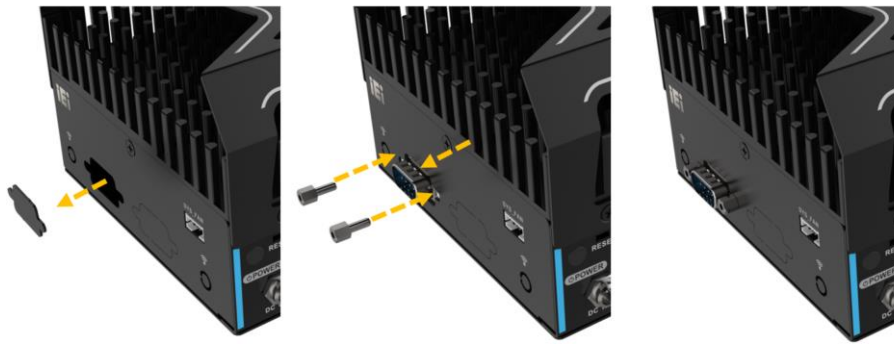


Figure 3-13: Knock out the reserved holes

3.6.3 iDPM Installation

Step 1: Locate the iDPM module slot.

Step 2: Remove the retention screw secured on the motherboard.

Step 3: Line up the notch on the module with the notch on the slot. Slide the iDPM module into the socket at an angle of about 20°

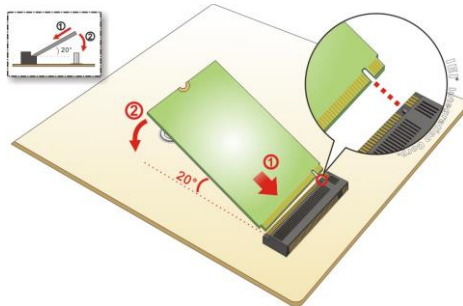


Figure 3-14: Inserting the M.2 Module into the Slot at an Angle

Step 4: Secure the iDPM module with the retention screw previously removed.

DRPC-W-TGL

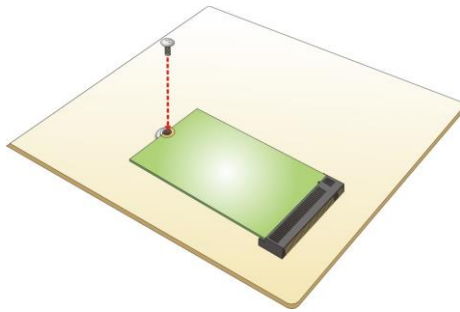


Figure 3-15: Securing the M.2 Module

Step 5: Connect the VGA cable to the VGA connector on the iDPM module.

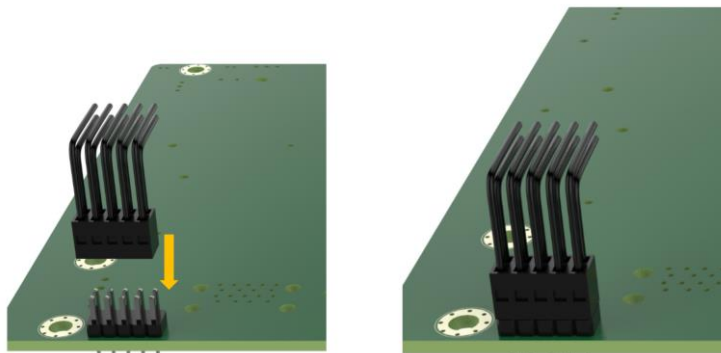


Figure 3-16: Connect the VGA cable to the VGA connector

Step 6: Knock out the reserved holes on the chassis and Secure the DB15 end of the VGA cable to the panel.



Figure 3-17: Knock out the reserved holes

3.7 Cover Installation

Install the cover, and fasten the 6 screws on the side



Figure 3-18: Install the cover

3.8 System Fan Installation (Optional)

When encountering high performance and high heat, additional cooling was needed. The optional external fan can help the DRPC-W-TGL Series solve the thermal problem.

To install the optional external fan, follow the steps below.

Step 1: Remove the 4 screws (2 on the front panel, 2 on the rear panel) on the DRPC-W-TGL Series as shown in the figure below.

Step 2: Install the expansion fan module (SF-DRPC-W-R10) to the DRPC-W-TGL Series, and secure it using the 4 screws removed previously.

Step 3: Connect the fan cable to the fan connector on the side panel.

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Figure 3-19: External Fan Module Installation

3.9 Mounting Brackets Installation

DRPC-W-TGL Series comes with DIN-RAIL mounting bracket, follow the steps below to install.

Step 1: Turn the embedded system over.

Step 2: Align the retention screw holes in each bracket with the corresponding retention screw holes on the bottom surface.

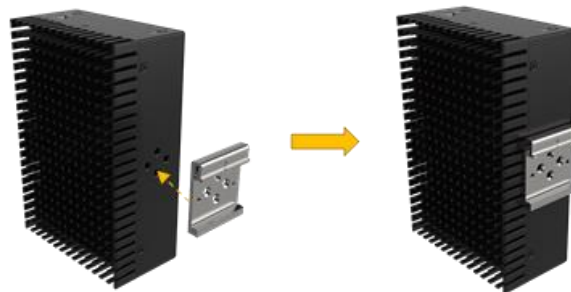


Figure 3-20: Align the retention screw holes

Step 3: Secure the brackets to the system by inserting retention screws into each bracket.

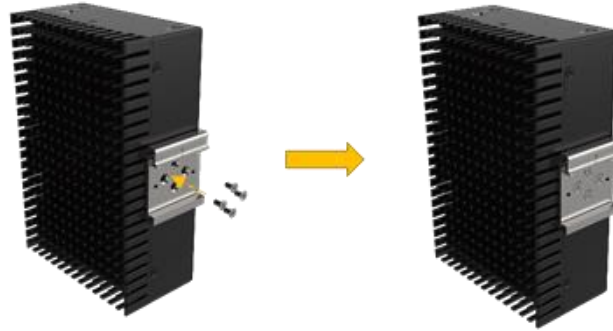


Figure 3-21: Secure the brackets

Step 4: Attach the upper edge of the mounting bracket at an angle. Push the system towards the DIN rail until mounting bracket hangs securely.

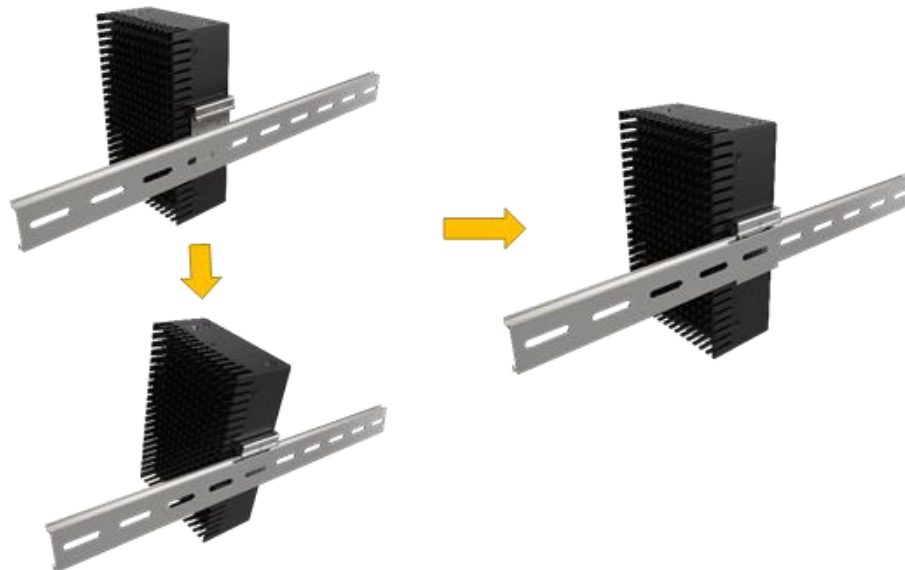


Figure 3-22: Mounting the system

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3.10 External Peripheral Interface Connectors

The DRPC-W-TGL Series has the following connectors. Detailed descriptions of the connectors can be found in the subsections below.

- Ethernet
- Power button
- Power DC jack
- HDMI
- DP
- USB

3.10.1 HDMI/DP Connector

To connect the HDMI/DP devices, please plug in HDMI/DP connector in the right direction as shown below:



Figure 3-23: HDMI/DP Connection

3.10.2 LAN Connectors

The LAN connectors allow connection to an external network

Step 1: Locate the RJ-45 connectors. The locations of the RJ-45 connectors are shown in **Chapter 1**

Step 2: Align the connectors. Align the RJ-45 connector on the LAN cable with one of the RJ-45 connectors on the DRPC-W-TGL Series.

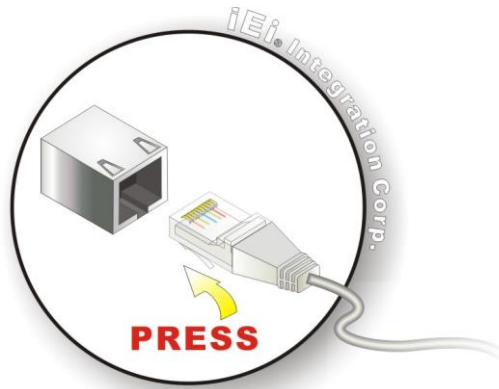


Figure 3-24: LAN Connection

Step 3: Insert the LAN cable RJ-45 connector. Once aligned, gently insert the LAN cable RJ-45 connector into the on-board RJ-45 connector

The RJ-45 Ethernet connector has two status LEDs, one green and one yellow. The green LED indicates activity on the port and the yellow LED indicates the port is linked. See



Figure 3-25: RJ-45 Ethernet Connector

| Activity/Link LED | | Speed LED | |
|-------------------|----------------|-----------|----------------------|
| STATUS | DESCRIPTION | STATUS | DESCRIPTION |
| Off | No link | Off | 10 Mbps connection |
| Yellow | Linked | Green | 1000 Mbps connection |
| Blinking | TX/RX activity | Orange | 2.5 Gbps connection |

Table 3-1: RJ-45 Ethernet Connector LEDs

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3.10.3 Power Connector

The power connector is a 2-pin DC jack connector on the front panel that can directly connect to a power adapter. The supported power input voltage is 12 VDC.

| Pin | Description |
|-----|-------------|
| 1 | 12V |
| 2 | GND |

Table 3-2: Power Connector Pinouts



Figure 3-26: Power Connector

3.10.4 USB 3.2 Gen 2 (10Gb/s) Connectors

The DRPC-W-TGL Series have four USB 3.2 ports. To connect a USB device, please follow the instructions below

Step 1: Located the USB connectors. The locations of the USB connectors are shown in **Chapter 1**

Step 2: Align the connectors. Align the USB device connector with one of the connectors on the I/O panel.

Step 3: Insert the device connector. Once aligned, gently insert the USB device connector into the onboard connector.

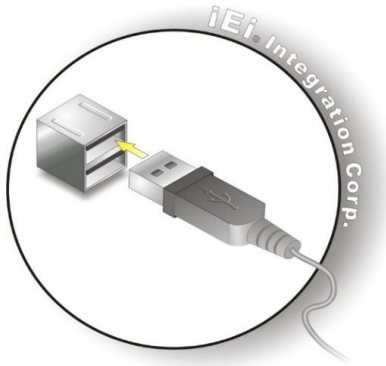


Figure 3-27: USB Connection

3.11 Internal Peripheral Interface Connectors (Optional)

3.11.1 Digital I/O Connector

- CN Label:** DIO1
- CN Type:** 14-pin header, p=2.00 mm
- CN Location:** See **Figure 3-28**
- CN Pinouts:** See **Table 3-3**

The 12-bit digital I/O connector provides programmable input and output for external devices.

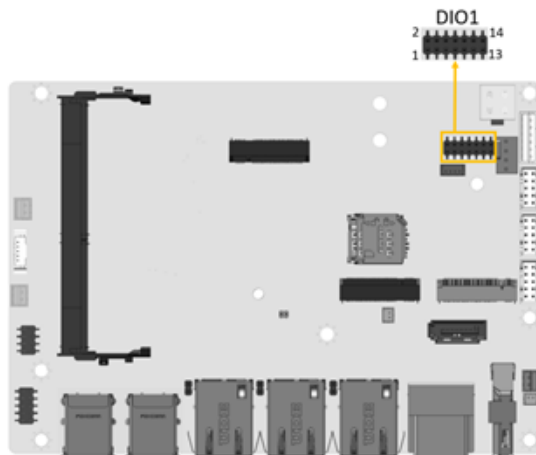


Figure 3-28: Digital I/O Connector Location

DRPC-W-TGL

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1 | GND | 2 | VCC |
| 3 | DOUT5 | 4 | DOUT4 |
| 5 | DOUT3 | 6 | DOUT2 |
| 7 | DOUT1 | 8 | DOUT0 |
| 9 | DIN5 | 10 | DIN4 |
| 11 | DIN3 | 12 | DIN2 |
| 13 | DIN1 | 14 | DIN0 |

Table 3-3: Digital I/O Connector Pinouts

3.11.2 M.2 Slot, B-key

- CN Label:** M2_1
- CN Type:** M.2 B-key slot
- CN Location:** See **Figure 3-29**
- CN Pinouts:** See **Table 3-4**

The M.2 B key (3042/2280) slot with PCIe Gen3 x2 and USB 2.0 signal supports NVMe storage or 5G module with SIM holder

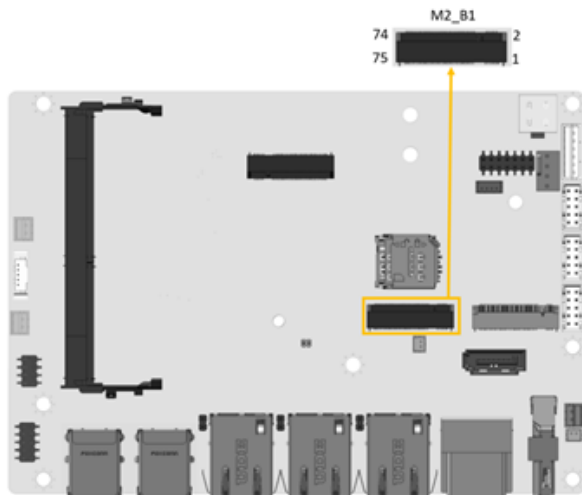


Figure 3-29: M.2 B key Slot Location

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|--------------|
| 1 | CONFIG_3 | 2 | +3.3V |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | POWER_OFF |
| 7 | USB_D+ | 8 | W_DISABLE |
| 9 | USB_D- | 10 | DAS/DSS# |
| 11 | GND | 12 | Module Key |
| 13 | Module Key | 14 | Module Key |
| 15 | Module Key | 16 | Module Key |
| 17 | Module Key | 18 | Module Key |
| 19 | Module Key | 20 | N/C |
| 21 | CONFIG_0 | 22 | N/C |
| 23 | N/C | 24 | N/C |
| 25 | N/C | 26 | GNSS_DISABLE |
| 27 | GND | 28 | N/C |
| 29 | PCIE_RXN1 | 30 | UIM_RST |
| 31 | PCIE_RXP1 | 32 | UIM_CLK |
| 33 | GND | 34 | UIM_DATA |
| 35 | PCIE_TXN1 | 36 | UIM_VCC |
| 37 | PCIE_TXP1 | 38 | DEVSLP |
| 39 | GND | 40 | N/C |
| 41 | PCIE_RXN0 | 42 | N/C |
| 43 | PCIE_RXP0 | 44 | N/C |
| 45 | GND | 46 | N/C |
| 47 | PCIE_TXN0 | 48 | N/C |
| 49 | PCIE_TXP0 | 50 | PERST# |
| 51 | GND | 52 | CLKREQ# |
| 53 | REFCLKN | 54 | PEWAKE |
| 55 | REFCLKP | 56 | N/C |
| 57 | GND | 58 | N/C |
| 59 | N/C | 60 | N/C |
| 61 | N/C | 62 | N/C |
| 63 | N/C | 64 | N/C |

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| | | | |
|----|----------|----|-------|
| 65 | N/C | 66 | N/C |
| 67 | WWAN_RST | 68 | N/C |
| 69 | PEDET | 70 | +3.3V |
| 71 | GND | 72 | +3.3V |
| 73 | GND | 74 | +3.3V |
| 75 | CONFIG_2 | | |

Table 3-4: M. 2 B key Slot Pinouts

3.11.3 M.2 Slot, A-key

- CN Label:** M2_A1
- CN Type:** M.2 A-key slot
- CN Location:** See **Figure 3-30**
- CN Pinouts:** See **Table 3-5**

The M.2 slot is keyed in the A position and accepts 2230 size of M.2 modules. The M.2 slot supports PCIe x2 and USB 2.0 signals.

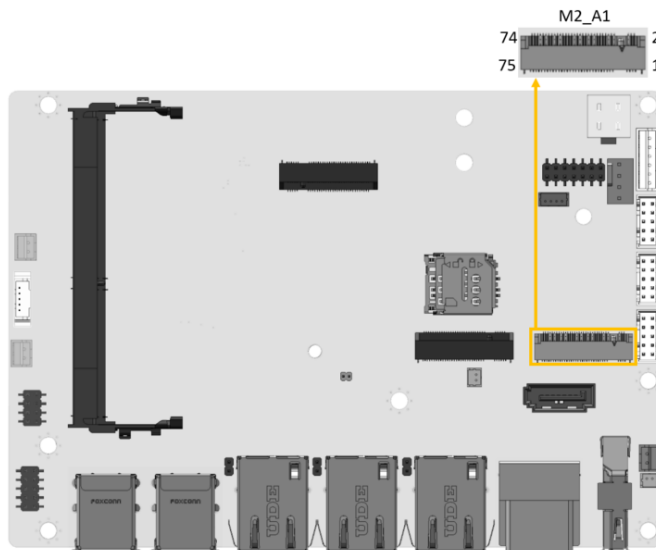


Figure 3-30: M.2 A-key Slot Location

| Pin | Description | Pin | Description |
|-----|--------------|-----|----------------|
| 1 | GND | 2 | +V3.3A |
| 3 | USB+ | 4 | +V3.3A |
| 5 | USB- | 6 | NC |
| 7 | GND | 8 | Module Key |
| 9 | Module Key | 10 | Module Key |
| 11 | Module Key | 12 | Module Key |
| 13 | Module Key | 14 | Module Key |
| 15 | Module Key | 16 | NC |
| 17 | NC | 18 | GND |
| 19 | NC | 20 | NC |
| 21 | NC | 22 | NC |
| 23 | GND | 24 | GND |
| 25 | NC | 26 | NC |
| 27 | NC | 28 | NC |
| 29 | GND | 30 | GND |
| 31 | NC | 32 | NC |
| 33 | GND | 34 | NC |
| 35 | PCIE_TX0+ | 36 | GND |
| 37 | PCIE_TX0- | 38 | NC |
| 39 | GND | 40 | NC |
| 41 | PCIE_RX0+ | 42 | NC |
| 43 | PCIE_RX0- | 44 | NC |
| 45 | GND | 46 | NC |
| 47 | CLK_PCIE0+ | 48 | NC |
| 49 | CLK_PCIE0- | 50 | NC |
| 51 | GND | 52 | BUF_PLT_RST# |
| 53 | PCIE_CLKREQ# | 54 | Pull Up +V3.3A |
| 55 | PCIE_WAKE# | 56 | Pull Up +V3.3A |
| 57 | GND | 58 | NC |
| 59 | PCIE_TX1+ | 60 | NC |
| 61 | PCIE_TX1- | 62 | NC |
| 63 | GND | 64 | NC |
| 65 | PCIE_RX1+ | 66 | NC |

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| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 67 | PCIE_RX1- | 68 | NC |
| 69 | GND | 70 | NC |
| 71 | CLK_PCIE1+ | 72 | +V3.3A |
| 73 | CLK_PCIE1- | 74 | +V3.3A |
| 75 | GND | | |

Table 3-5: M.2 A-Key Slot Pinouts

3.11.4 USB 2.0 Connector

- CN Label:** USB3
- CN Type:** 8-pin header, p=2.00 mm
- CN Location:** See **Figure 3-31**
- CN Pinouts:** See **Table 3-6**

The USB connector provides two USB 2.0 ports by dual-port USB cable.

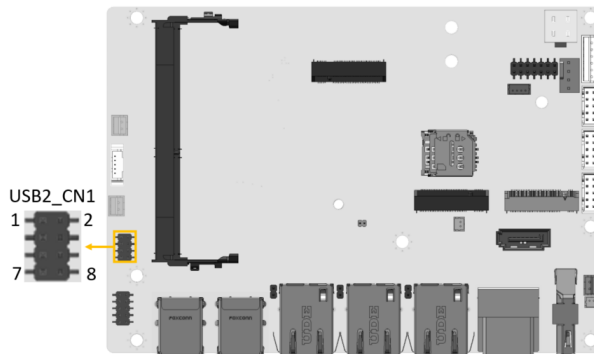


Figure 3-31: USB Connector Location

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1 | VCC | 2 | GND |
| 3 | USB DATA- | 4 | USB DATA+ |
| 5 | USB DATA+ | 6 | USB DATA- |
| 7 | GND | 8 | VCC |

Table 3-6: USB Connector Pinouts

3.11.5 IDPM1 Display Connector

- CN Label:** IDPM
- CN Type:** 75-pin slot, p=0.5 mm
- CN Location:** See **Figure 3-32**
- CN Pinouts:** See **Table 3-7**

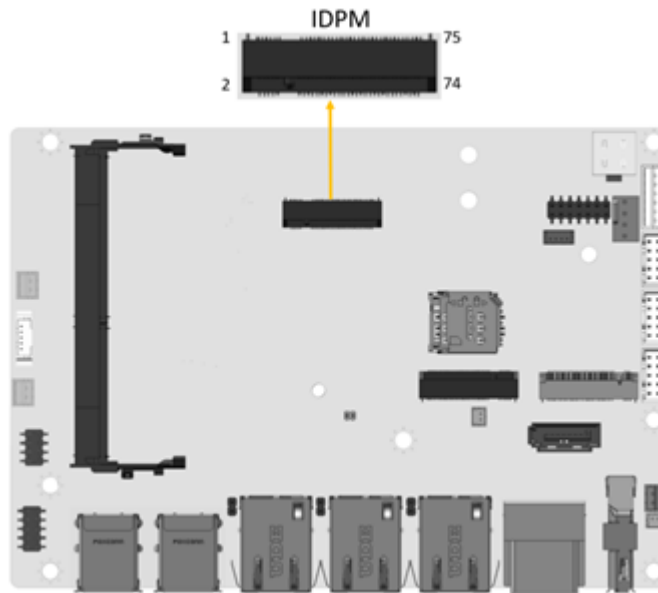


Figure 3-32: iDPM Slot Location

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|----------------|----------------------|----------------|--------------------|
| 1 | GND | 2 | +3.3V |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | +3.3V |
| 7 | GND | 8 | +3.3V |
| 9 | GND | 10 | +3.3V |
| 11 | +5V | 12 | Module Key |
| 13 | Module Key | 14 | Module Key |
| 15 | Module Key | 16 | Module Key |
| 17 | Module Key | 18 | Module Key |
| 19 | Module Key | 20 | +3.3VS |
| 21 | DISPLAY_DETECT_PIN21 | 22 | +3.3VS |

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| | | | |
|----|----------------------|----|----------------|
| 23 | DISPLAY_DETECT_PIN23 | 24 | +3.3VS |
| 25 | GND | 26 | +3.3VS |
| 27 | GND | 28 | GND |
| 29 | EDP_TX3_DN | 30 | +12VS |
| 31 | EDP_TX3_DP | 32 | +12VS |
| 33 | GND | 34 | +12VS |
| 35 | EDP_TX2_DN | 36 | +12VS |
| 37 | EDP_TX2_DP | 38 | GND |
| 39 | GND | 40 | SMB_CLK |
| 41 | EDP_TX1_DN | 42 | SMB_DATA |
| 43 | EDP_TX1_DP | 44 | GND |
| 45 | GND | 46 | EC_BKLT_CTRL |
| 47 | EDP_TX0_DN | 48 | EDP1_BKLT_CTRL |
| 49 | EDP_TX0_DP | 50 | EDP1_BKLT_EN |
| 51 | GND | 52 | EDP1_VDD_EN # |
| 53 | EDP_AUX_DN | 54 | EDP_HPD_R |
| 55 | EDP_AUX_DP | 56 | BUF_PLT_RST# |
| 57 | GND | 58 | LVDS_EN |
| 59 | GND | 60 | +V5S |
| 61 | GND | 62 | +V5S |
| 63 | GND | 64 | +V5S |
| 65 | GND | 66 | +V5S |
| 67 | GND | 68 | +12VA |
| 69 | GND | 70 | +12VA |
| 71 | GND | 72 | +12VA |
| 73 | GND | 74 | +12VA |
| 75 | GND | | |

Table 3-7: iDPM Connector Pinouts

3.11.6 Audio Connector

- CN Label:** IAUDIO1
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-33**
- CN Pinouts:** See **Table 3-8**

The audio connector is connected to external audio devices (AC-KIT-888S-R10) including speakers and microphones for the input and output of audio signals to and from the system.

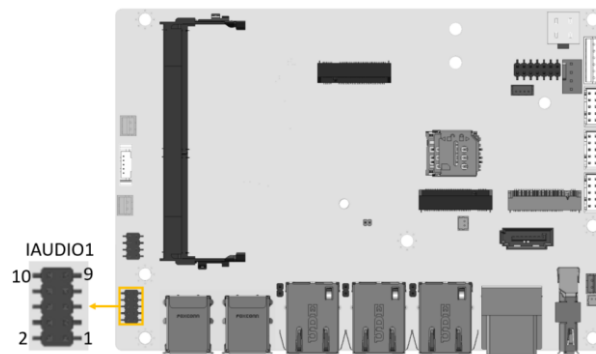


Figure 3-33: Audio Connector Location

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|---------------|
| 1 | HDA_SYNC_R | 2 | HDA_BIT_CLK_R |
| 3 | HDA_SDOUT_R | 4 | HDA_PCBEEP_R |
| 5 | HDA_SDIN_R | 6 | HDA_RST#_R |
| 7 | P5V | 8 | GND |
| 9 | P12V | 10 | GND |

Table 3-8: Audio Connector Pinouts

DRPC-W-TGL

3.12 Powering On/Off the System

**WARNING:**

Make sure a power supply with the correct input voltage is being fed into the system. Incorrect voltages applied to the system may cause damage to the internal electronic components and may also cause injury to the user.

The power of the system needs more than 12V5A

Step 1: Connect the power source to the power input jack.

Step 2: Push the power button the power LED indicator should turn on.

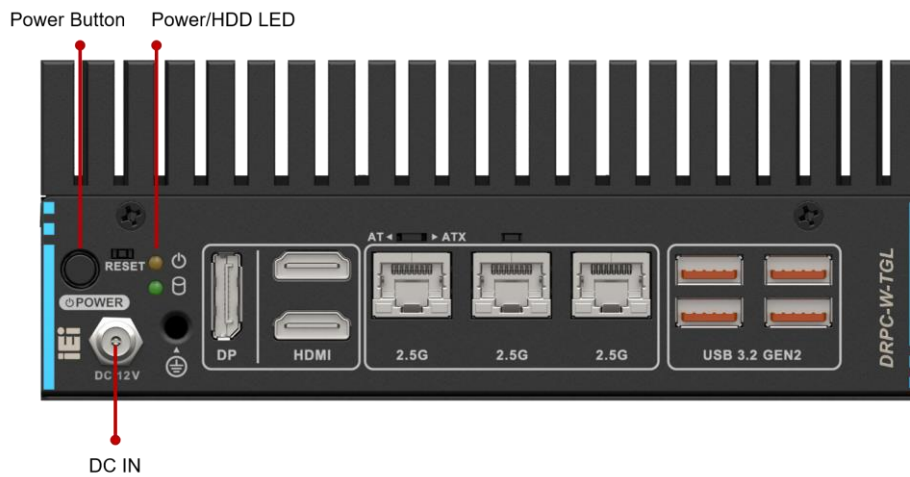


Figure 3-34: Power Input & Button & LED

- **Power on** the system: press the power button for 1 seconds
- **Power off** the system: press the power button for 6 seconds

Power Button

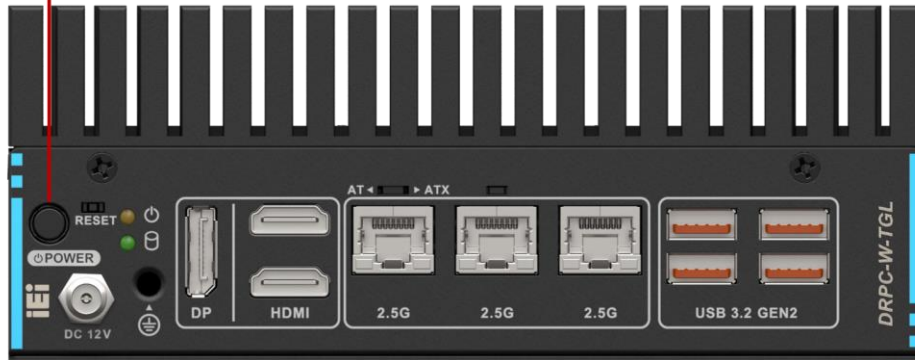


Figure 3-35: Power Button

3.13 Available Drivers

All the drivers for the DRPC-W-TGL Series are available on IEI Resource Download Center (<https://download.ieiworld.com>). Type DRPC-W-TGL Series and press Enter to find all the relevant software, utilities, and documentation.

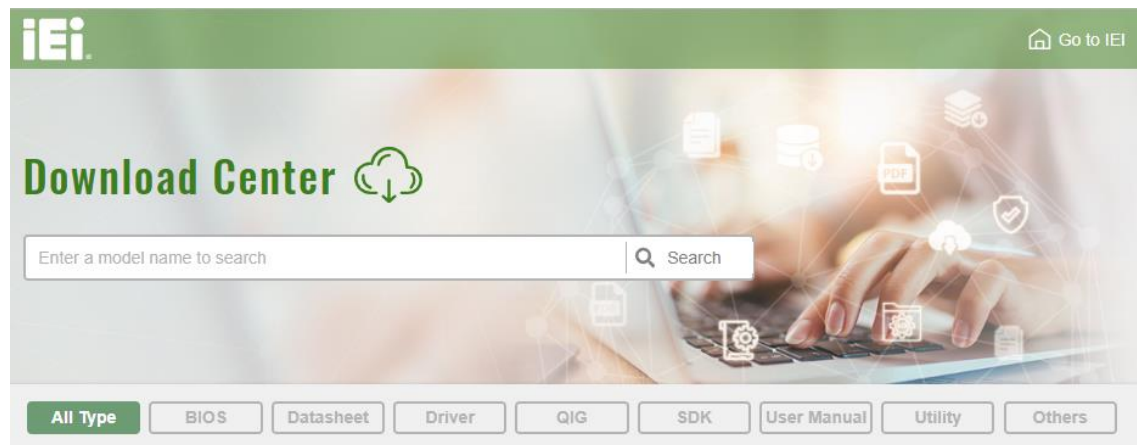


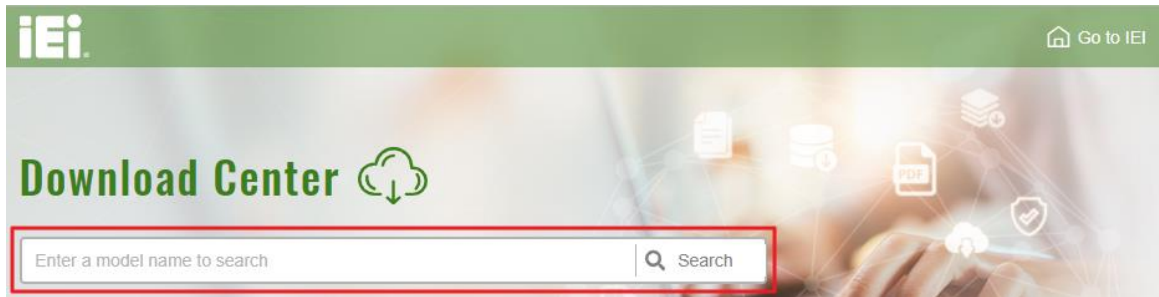
Figure 3-36: IEI Resource Download Center

DRPC-W-TGL

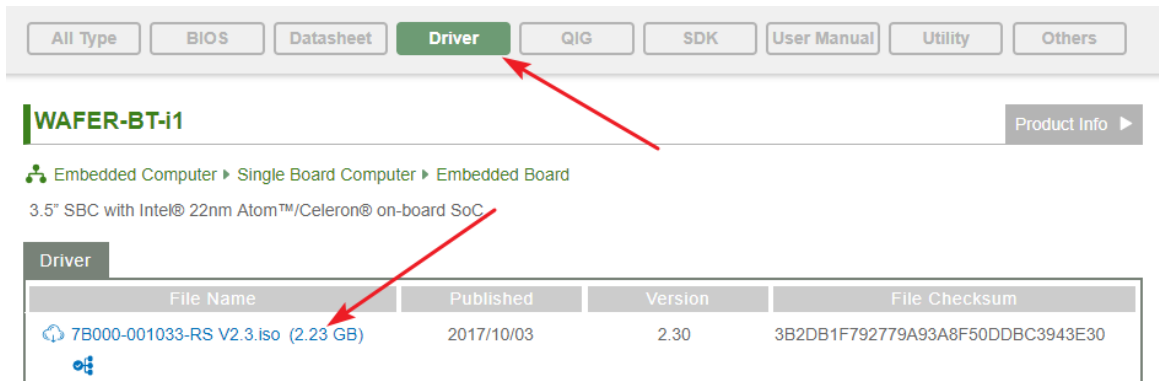
3.13.1 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

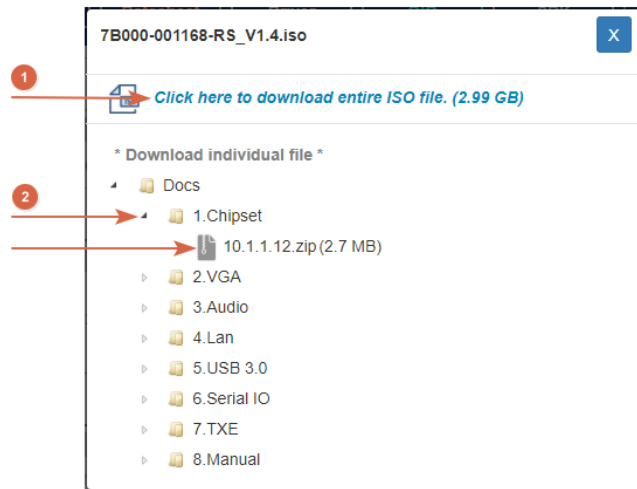
Step 1: Go to <https://download.ieiworld.com>. Type DRPC-W-TGL Series and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).

**NOTE:**

To install software from the downloaded ISO image file in Windows 10 (or later), double-click the ISO file to mount it as a virtual drive to view its content.

3.14 Maintenance

To configure the jumper settings, please follow the steps below.

Step 1: Remove the top cover. See **Figure 3-1**.

Step 2: Locate the jumper on the embedded motherboard.

Step 3: Make the jumper settings in accordance with the settings described and defined in the following sections.

DRPC-W-TGL

3.14.1 Flash Descriptor Security Override Jumper

- CN Label:** ME_FLASH1
- CN Type:** 2-pin header, P=1.27mm
- CN Location:** See **Figure 3-37**
- CN Pinouts:** See **Table 3-9**

The ME_FLASH1 connector is used for Flash Descriptor Security Override or ME Debug Mode

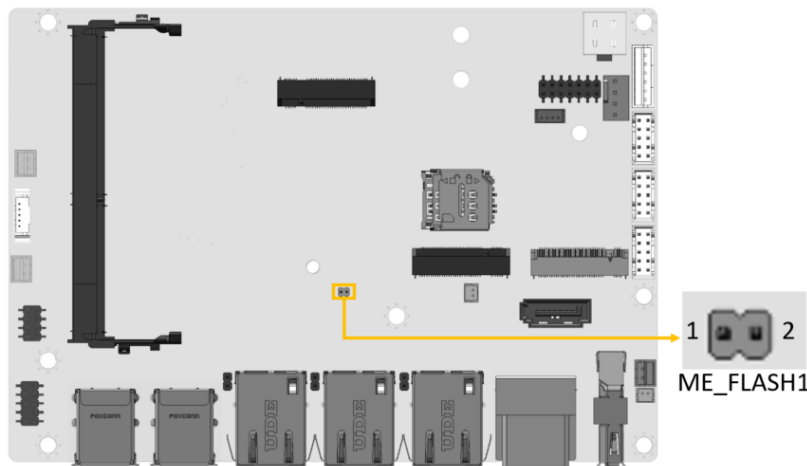


Figure 3-37: ME Override Setting Jumper Locations

| Setting | Description |
|---------|--------------------|
| Open | Disabled (Default) |
| Short | Enabled |

Table 3-9: ME Override Setting Jumper Pinouts

To update the ME firmware, please follow the steps below

Step 1: Before turning on the system power, short the Flash Descriptor Security Override jumper.

Step 2: Update the BIOS and ME firmware, and then turn off the system power.

Step 3: Remove the metal clip on the Flash Descriptor Security Override jumper to its default setting

Step 4: Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update

3.14.2 Clear CMOS Button

- CN Label:** J_CMOS1
- CN Type:** Button
- CN Location:** See **Figure 3-38**
- CN Pinouts:** See **Table 3-10**

To clear the CMOS Setup (for example if you have forgotten the password, you should clear the CMOS and then reset the password), you should disconnect the RTC battery and press the button for about 3 seconds. This will set back to normal operation mode.

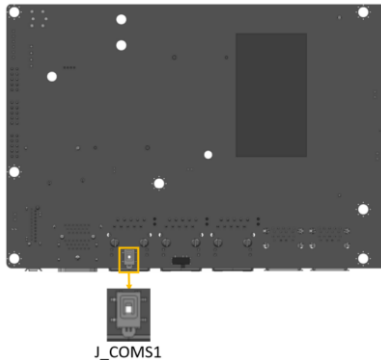


Figure 3-38: Clear CMOS Location

| PIN NO. | DESCRIPTION |
|----------------|---------------------------------------|
| NC (default) | Keep CMOS Setup (Normal Operation) |
| Press button | Clear CMOS Setup |

Table 3-10: Clear CMOS Pinouts

DRPC-W-TGL**3.14.3 AT/ATX Power Mode Setting**

CN Label: J_ATX_AT1
CN Type: 3-pin switch
CN Pinouts: See **Table 3-11**

The AT/ATX power mode selection is made through the AT/ATX power mode switch which is shown in.

| PIN NO. | DESCRIPTION |
|----------------|--------------------------|
| Short A - B | ATX Power Mode (default) |
| Short B - C | AT Power Mode |

Table 3-11: AT/ATX Power Mode Switch Pinouts

Chapter

4

System Motherboard

DRPC-W-TGL

4.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

4.1.1 DRPC-W-TGL Series Layout

The figures below show all the connectors and jumpers.

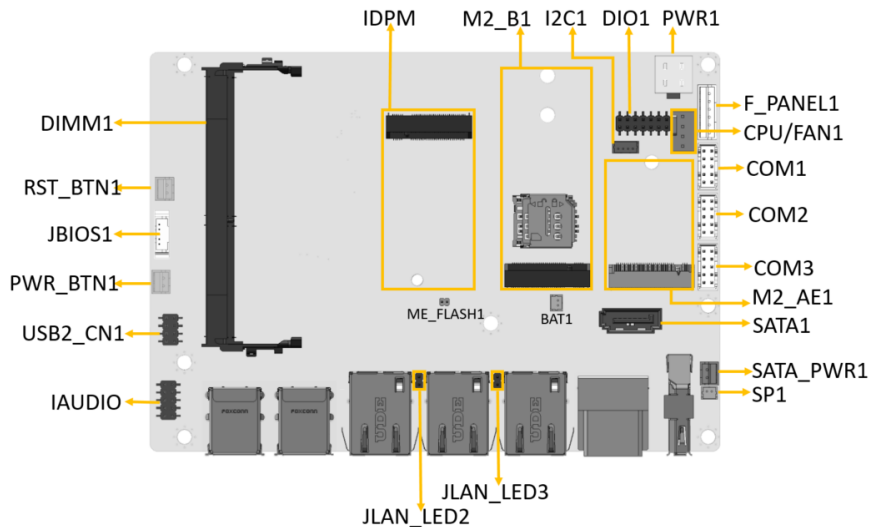


Figure 4-1: Connector and Jumper Locations

4.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

| Connector | Type | Label |
|-----------------------|---------------|-------------------------|
| Audio connector | 10-pin header | IAUDIO |
| Battery connector | 2-pin wafer | BAT1 |
| Digital I/O connector | 14-pin header | DIO1 |
| Fan connector | 4-pin wafer | CPU/FAN1 |
| Front panel connector | 6-pin wafer | F_PANEL1 |
| LAN LED connector | 2-pin header | JLAN_LED2, JLAN_LED3 |
| iDPM connector | 75-pin slot | IDPM |

| | | |
|--------------------------------------|----------------------|------------|
| M.2 2230 A-key slot | M.2 A-key slot | M2_AE1 |
| M.2 3052/2042 B-key slot | M.2 B-key slot | M2_B1 |
| Memory module slot | 260-pin DDR4 SO-DIMM | DIMM1 |
| Power connector | 4-pin Molex | PWR1 |
| Power button connector | 2-pin wafer | PWR_BTN1 |
| Reset button connector | 2-pin wafer | RST_BTN1 |
| RS-232 serial port connector | 10-pin header | COM1 |
| RS-232/422/485 serial port connector | 10-pin header | COM2, COM3 |
| Serial ATA connector | 7-pin SATA connector | SATA1 |
| SATA power connector | 2-pin wafer | SATA_PWR1 |
| SMBus/I ² C connector | 4-pin wafer | I2C1 |
| USB 2.0 connector | 8-pin header | USB2_CN1 |

Table 4-1: Peripheral Interface Connectors

4.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

| Connector | Type | Label |
|--------------------------|---------------|--------------------|
| HDMI connector | HDMI | HDMI1 |
| DP connector | DP | DP1 |
| LAN connectors | RJ-45 | LAN1, LAN2, LAN3 |
| USB 3.2 Gen 2 connectors | USB 3.2 Gen 2 | USB_CON1, USB_CON2 |

Table 4-2: Rear Panel Connectors

DRPC-W-TGL

4.2 Internal Peripheral Connectors

The section describes all of the connectors on the DRPC-W-TGL Series.

4.2.1 Battery Connector



CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.



NOTE:

It is recommended to attach the RTC battery onto the system chassis in which the DRPC-W-TGL Series is installed.

| | |
|---------------------|------------------------|
| CN Label: | BAT1 |
| CN Type: | 2-pin wafer, p=1.25 mm |
| CN Location: | See Figure 4-2 |
| CN Pinouts: | See Table 4-3 |

The battery connector is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

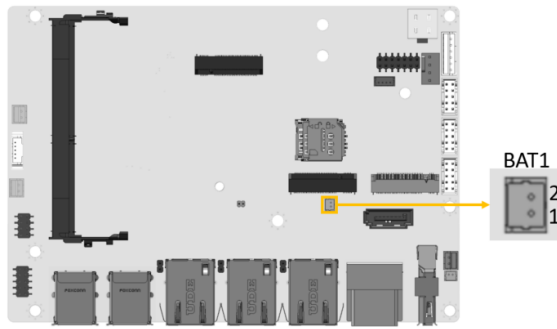


Figure 4-2: Battery Connector Location

| Pin | Description |
|------------|--------------------|
| 1 | VBAT+ |
| 2 | GND |

Table 4-3: Battery Connector Pinouts

DRPC-W-TGL

4.2.2 Digital I/O Connector

- CN Label:** DIO1
- CN Type:** 14-pin header, p=2.00 mm
- CN Location:** See **Figure 4-3**
- CN Pinouts:** See **Table 4-4**

The 12-bit digital I/O connector provides programmable input and output for external devices.

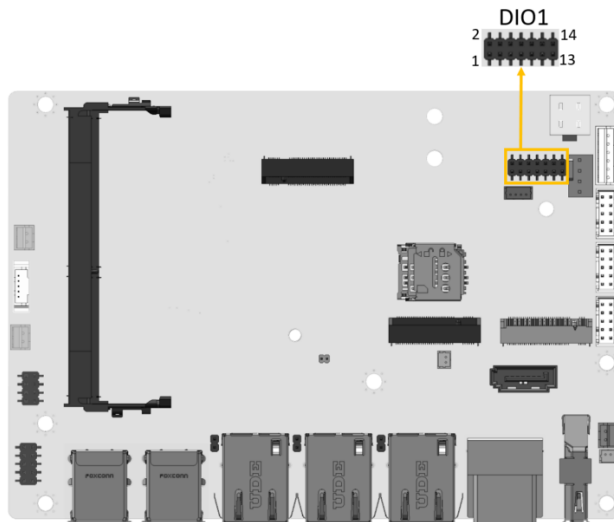


Figure 4-3: Digital I/O Connector Location

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1 | GND | 2 | VCC |
| 3 | DOUT5 | 4 | DOUT4 |
| 5 | DOUT3 | 6 | DOUT2 |
| 7 | DOUT1 | 8 | DOUT0 |
| 9 | DIN5 | 10 | DIN4 |
| 11 | DIN3 | 12 | DIN2 |
| 13 | DIN1 | 14 | DIN0 |

Table 4-4: Digital I/O Connector Pinouts

4.2.3 Fan Connector

- CN Label:** CPU/FAN1
- CN Type:** 4-pin wafer, p=2.54 mm
- CN Location:** See **Figure 4-4**
- CN Pinouts:** See **Table 4-5**

The fan connector attaches to a smart cooling fan.

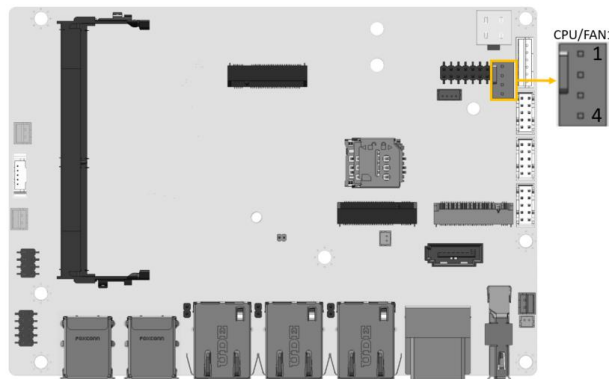


Figure 4-4: Fan Connector Location

| Pin | Description |
|-----|-------------|
| 1 | GND |
| 2 | +12V |
| 3 | FANIO |
| 4 | PWM |

Table 4-5: Fan Connector Pinouts

DRPC-W-TGL

4.2.4 Front Panel Connector

- CN Label:** F_PANEL1
- CN Type:** 6-pin wafer, p=2.00 mm
- CN Location:** See **Figure 4-5**
- CN Pinouts:** See **Table 4-6**

The front panel connector connects to the power LED indicator and HDD LED indicator on the system front panel.

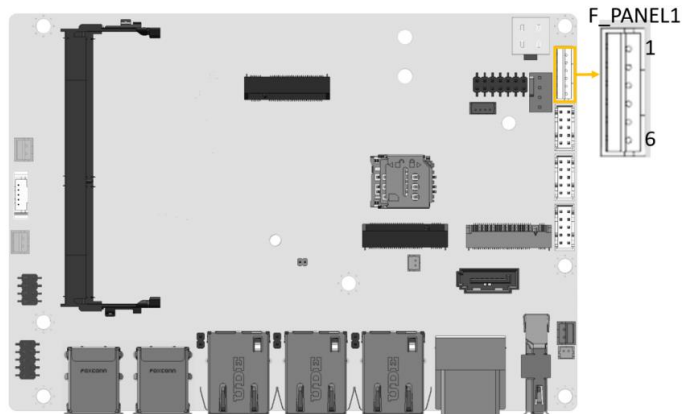


Figure 4-5: Front Panel Connector Location

| Pin | Description |
|------------|--------------------|
| 1 | VCC |
| 2 | GND |
| 3 | PWR_LED+ |
| 4 | PWR_LED- |
| 5 | HDD_LED+ |
| 6 | HDD_LED- |

Table 4-6: Front Panel Connector Pinouts

4.2.5 LAN LED Connectors

CN Label: JLAN_LED2, JLAN_LED3

CN Type: 2-pin header, p=2.00 mm

CN Location: See **Figure 4-6**

CN Pinouts: See **Table 4-7**

The LAN LED connectors connect to the LAN link LEDs on the system.

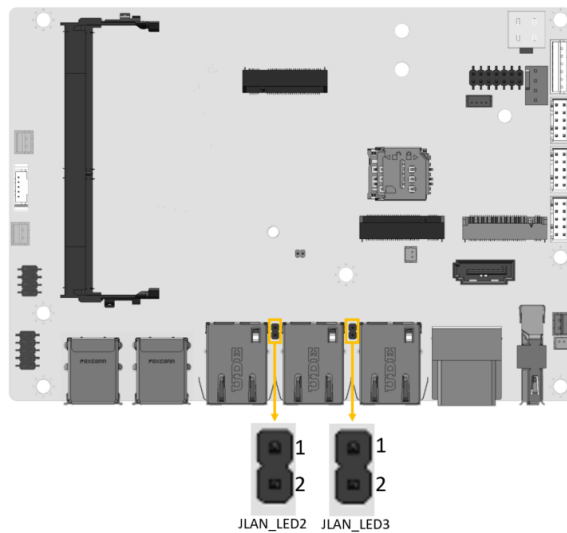


Figure 4-6: LAN LED Connector Locations

| Pin | Description |
|-----|-------------------|
| 1 | +3.3V |
| 2 | LAN1_LED_LNK#_ACT |

Table 4-7: LAN LED Connector Pinouts

DRPC-W-TGL

4.2.6 iDPM Connector

- CN Label:** IDPM
- CN Type:** 75-pin slot, p=0.5 mm
- CN Location:** See **Figure 4-7**
- CN Pinouts:** See **Table 4-8**

The iDPM slot only use for IEI eDP/LVDS/VGA module

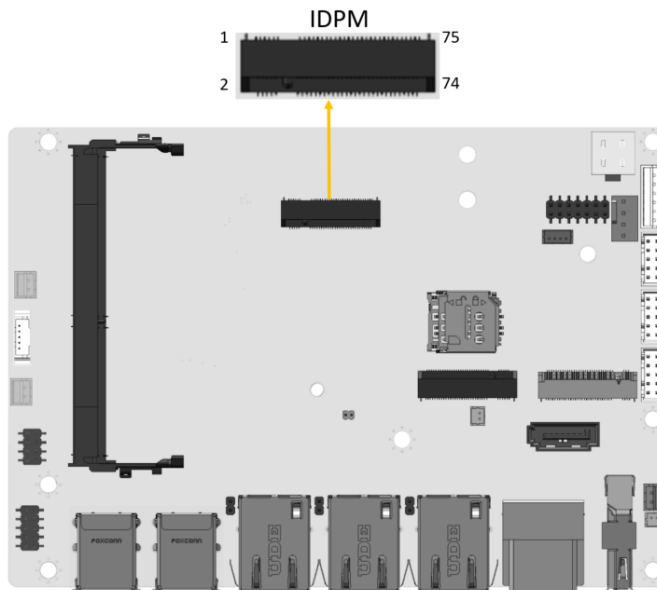


Figure 4-7: iDPM Connector Location

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1 | GND | 2 | +3.3V |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | +3.3V |
| 7 | GND | 8 | +3.3V |
| 9 | GND | 10 | +3.3V |
| 11 | +5V | 12 | Module Key |
| 13 | Module Key | 14 | Module Key |
| 15 | Module Key | 16 | Module Key |
| 17 | Module Key | 18 | Module Key |

| Pin | Description | Pin | Description |
|-----|--------------------------|-----|----------------|
| 19 | Module Key | 20 | +3.3VS |
| 21 | DISPLAY_DETECT_P IN21 | 22 | +3.3VS |
| 23 | DISPLAY_DETECT_P IN23 | 24 | +3.3VS |
| 25 | GND | 26 | +3.3VS |
| 27 | GND | 28 | GND |
| 29 | EDP_TX3_DN | 30 | +12VS |
| 31 | EDP_TX3_DP | 32 | +12VS |
| 33 | GND | 34 | +12VS |
| 35 | EDP_TX2_DN | 36 | +12VS |
| 37 | EDP_TX2_DP | 38 | GND |
| 39 | GND | 40 | SMB_CLK |
| 41 | EDP_TX1_DN | 42 | SMB_DATA |
| 43 | EDP_TX1_DP | 44 | GND |
| 45 | GND | 46 | EC_BKLT_CTRL |
| 47 | EDP_TX0_DN | 48 | EDP1_BKLT_CTRL |
| 49 | EDP_TX0_DP | 50 | EDP1_BKLT_EN |
| 51 | GND | 52 | EDP1_VDD_EN # |
| 53 | EDP_AUX_DN | 54 | EDP_HPD_R |
| 55 | EDP_AUX_DP | 56 | BUF_PLT_RST# |
| 57 | GND | 58 | LVDS_EN |
| 59 | GND | 60 | +V5S |
| 61 | GND | 62 | +V5S |
| 63 | GND | 64 | +V5S |
| 65 | GND | 66 | +V5S |
| 67 | GND | 68 | +12VA |
| 69 | GND | 70 | +12VA |
| 71 | GND | 72 | +12VA |
| 73 | GND | 74 | +12VA |
| 75 | GND | | |

Table 4-8: iDPM Connector Pinouts

DRPC-W-TGL

4.2.7 M.2 Slot, B-key

- CN Label:** M2_B1
- CN Type:** M.2 B-key slot
- CN Location:** See **Figure 4-8**
- CN Pinouts:** See **Table 4-9**

The M.2 slot is keyed in the B position and accepts 3052/2242 size of M.2 modules. The M.2 slot supports PCIe x2 and USB 2.0 signals.

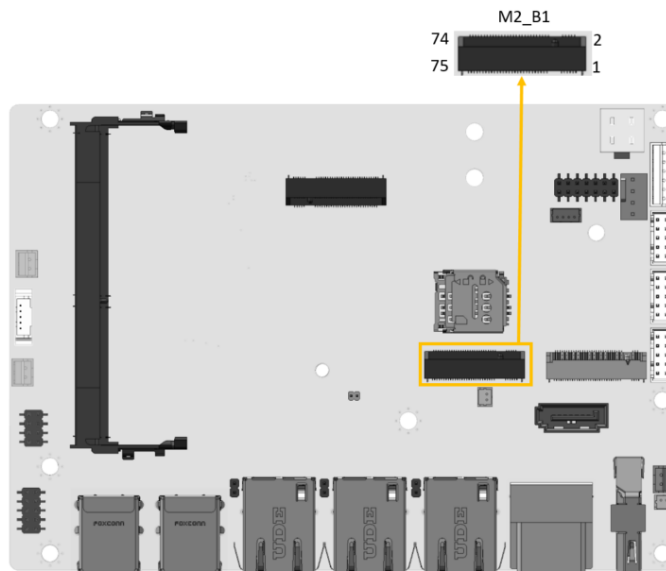


Figure 4-8: M.2 B-key Slot Location

| Pin | Description | Pin | Description |
|-----|-------------|-----|--------------|
| 1 | CONFIG_3 | 2 | +3.3V |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | WWAN_FCP_OFF |
| 7 | USB_D+ | 8 | WWAN_DISABLE |
| 9 | USB_D- | 10 | NC |
| 11 | GND | 12 | Module Key |
| 13 | Module Key | 14 | Module Key |
| 15 | Module Key | 16 | Module Key |

| Pin | Description | Pin | Description |
|-----|-------------|-----|---------------|
| 17 | Module Key | 18 | Module Key |
| 19 | Module Key | 20 | NC |
| 21 | CONFIG_0 | 22 | NC |
| 23 | NC | 24 | NC |
| 25 | NC | 26 | NC |
| 27 | GND | 28 | NC |
| 29 | PCIE_RXN5 | 30 | WWAN_UIM_RST |
| 31 | PCIE_RXP5 | 32 | WWAN_UIM_CLK |
| 33 | GND | 34 | WWAN_UIM_DATA |
| 35 | PCIE_TXN5 | 36 | UIM_PWR |
| 37 | PCIE_TXP5 | 38 | DEVSLP |
| 39 | GND | 40 | NC |
| 41 | PCIE_RXN4 | 42 | NC |
| 43 | PCIE_RXP4 | 44 | NC |
| 45 | GND | 46 | NC |
| 47 | PCIE_TXN4 | 48 | NC |
| 49 | PCIE_TXP4 | 50 | BUF_PLT_RST# |
| 51 | GND | 52 | N/C |
| 53 | REFCLKN | 54 | PCIE_WAKE# |
| 55 | REFCLKP | 56 | NC |
| 57 | GND | 58 | NC |
| 59 | NC | 60 | NC |
| 61 | NC | 62 | NC |
| 63 | NC | 64 | NC |
| 65 | NC | 66 | NC |
| 67 | WWAN_RST | 68 | NC |
| 69 | GND | 70 | +3.3V |
| 71 | GND | 72 | +3.3V |
| 73 | GND | 74 | +3.3V |
| 75 | GND | | |

Table 4-9: M.2 B-Key Slot Pinouts

DRPC-W-TGL

4.2.8 M.2 Slot, A-key

- CN Label:** M2_A1
- CN Type:** M.2 A-key slot
- CN Location:** See **Figure 4-9**
- CN Pinouts:** See **Table 4-10**

The M.2 slot is keyed in the A position and accepts 2230 size of M.2 modules. The M.2 slot supports PCIe x1 and USB 2.0 signals.

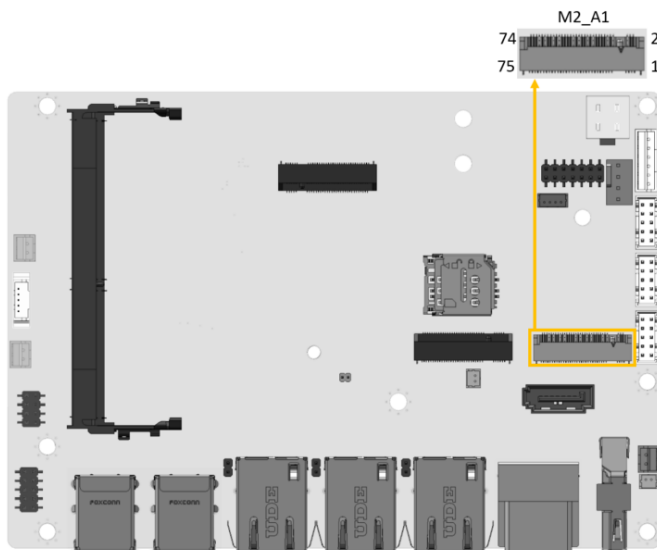


Figure 4-9: M.2 A-key Slot Location

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1 | GND | 2 | +V3.3A |
| 3 | USB+ | 4 | +V3.3A |
| 5 | USB- | 6 | NC |
| 7 | GND | 8 | Module Key |
| 9 | Module Key | 10 | Module Key |
| 11 | Module Key | 12 | Module Key |
| 13 | Module Key | 14 | Module Key |
| 15 | Module Key | 16 | NC |
| 17 | NC | 18 | GND |

| Pin | Description | Pin | Description |
|-----|-------------|-----|----------------|
| 19 | NC | 20 | NC |
| 21 | NC | 22 | NC |
| 23 | GND | 24 | GND |
| 25 | NC | 26 | NC |
| 27 | NC | 28 | NC |
| 29 | GND | 30 | GND |
| 31 | NC | 32 | NC |
| 33 | GND | 34 | NC |
| 35 | PCIE_TX9+ | 36 | GND |
| 37 | PCIE_TX9- | 38 | CL_RST# |
| 39 | GND | 40 | CL_DATA |
| 41 | PCIE_RX9+ | 42 | CL_CLK |
| 43 | PCIE_RX9- | 44 | NC |
| 45 | GND | 46 | NC |
| 47 | CLK_M2_A+ | 48 | NC |
| 49 | CLK_M2_A- | 50 | NC |
| 51 | GND | 52 | BUF_PLT_RST# |
| 53 | NC | 54 | Pull Up +V3.3A |
| 55 | NC | 56 | Pull Up +V3.3A |
| 57 | GND | 58 | NC |
| 59 | NC | 60 | NC |
| 61 | NC | 62 | NC |
| 63 | GND | 64 | NC |
| 65 | NC | 66 | NC |
| 67 | NC | 68 | NC |
| 69 | GND | 70 | NC |
| 71 | NC | 72 | +V3.3A |
| 73 | NC | 74 | +V3.3A |
| 75 | GND | | |

Table 4-10: M.2 A-Key Slot Pinouts

DRPC-W-TGL**4.2.9 DDR4 SO-DIMM Socket**

- CN Label:** DIMM1
- CN Type:** 260-pin DDR4 SO-DIMM socket
- CN Location:** See **Figure 4-10**

The SO-DIMM slot is for installing the DDR4 SO-DIMM.

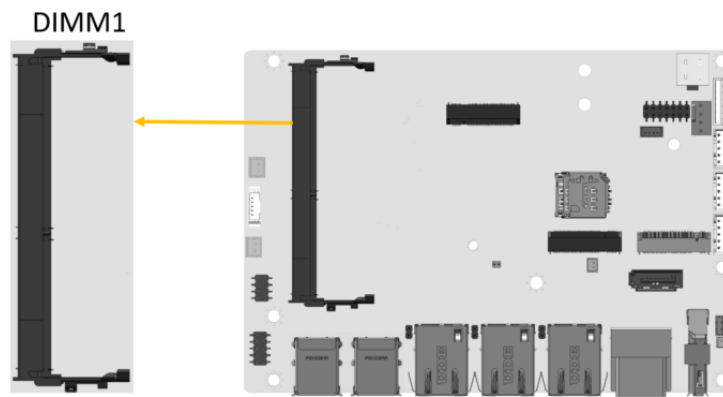


Figure 4-10: DDR4 SO-DIMM Socket Location

4.2.10 Power Connector

- CN Label:** PWR1
- CN Type:** 4-pin Molex, p=4.2 mm
- CN Location:** See **Figure 4-11**
- CN Pinouts:** See **Table 4-11**

The connector supports the +12V power supply.

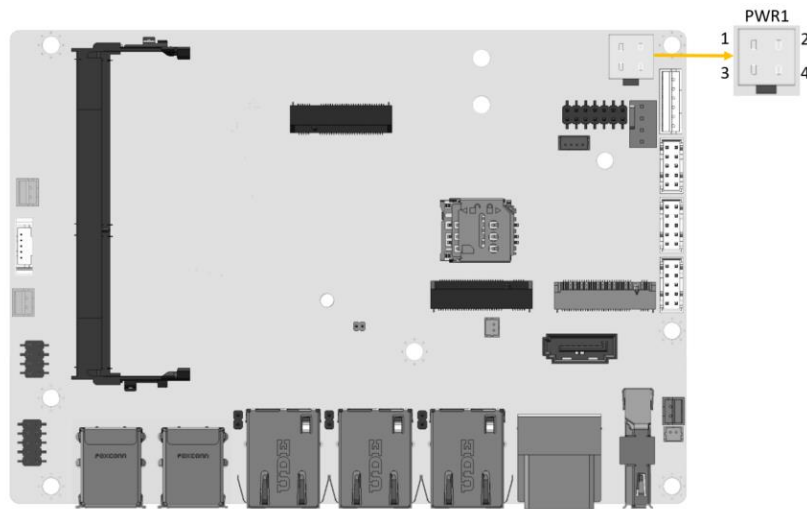


Figure 4-11: +12V DC-IN Power Connector Location

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|----------------|--------------------|----------------|--------------------|
| 1 | GND | 2 | GND |
| 3 | +12V | 4 | +12V |

Table 4-11: +12V DC-IN Power Connector Pinouts

DRPC-W-TGL

4.2.11 Power Button Connector

- CN Label:** PWR_BTN1
- CN Type:** 2-pin wafer, p=2.00 mm
- CN Location:** See **Figure 4-12**
- CN Pinouts:** See **Table 4-12**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

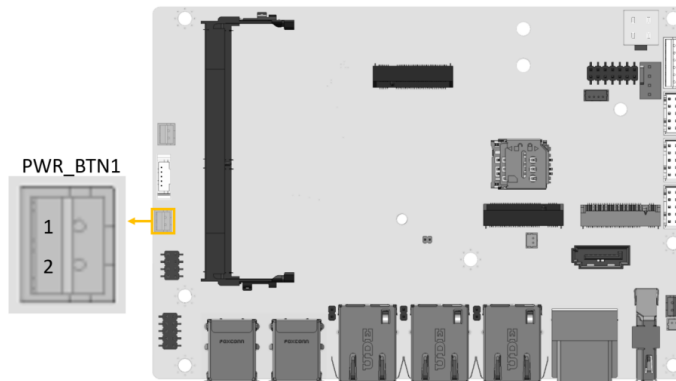


Figure 4-12: Power Button Connector Location

| Pin | Description |
|-----|-------------|
| 1 | PWR_BTN+ |
| 2 | PWR_BTN- |

Table 4-12: Power Button Connector Pinouts

4.2.12 Reset Button Connector

- CN Label:** RST_BTN1
- CN Type:** 2-pin wafer, p=2.00 mm
- CN Location:** See **Figure 4-13**
- CN Pinouts:** See **Table 4-13**

The reset button connector is connected to a reset switch on the system chassis to enable users to reboot the system when the system is turned on.

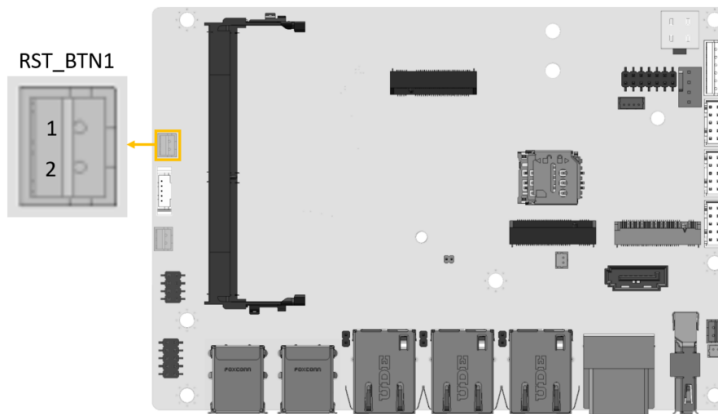


Figure 4-13: Reset Button Connector Location

| Pin | Description |
|-----|-------------|
| 1 | RESET+ |
| 2 | RESET- |

Table 4-13: Reset Button Connector Pinouts

DRPC-W-TGL

4.2.13 RS-232 Serial Port Connector

- CN Label:** COM1
- CN Type:** 10-pin header, p=2.0 mm
- CN Location:** See **Figure 4-14**
- CN Pinouts:** See **Table 4-14**

The serial connector provides RS-232 connection.

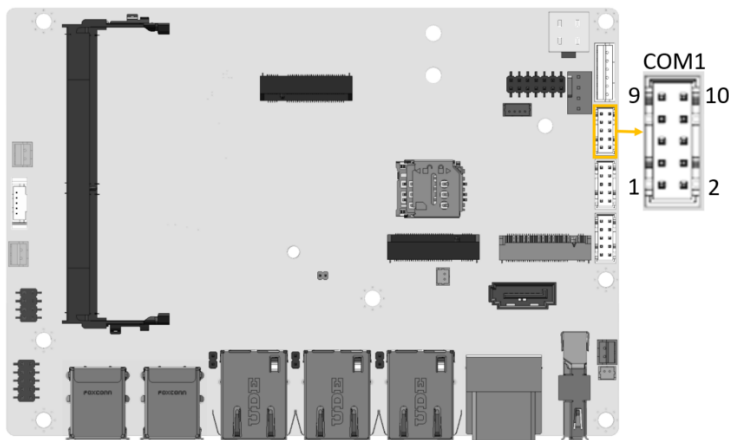


Figure 4-14: RS-232 Serial Port Connector Location

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|----------------|--------------------|----------------|--------------------|
| 1 | DCD | 2 | DSR |
| 3 | RXD | 4 | RTS |
| 5 | TXD | 6 | CTS |
| 7 | DTR | 8 | RI |
| 9 | GND | 10 | GND |

Table 4-14: RS-232 Serial Port Connector Pinouts

4.2.14 RS-232/422/485 Serial Port Connector

- CN Label:** COM2, COM3
- CN Type:** 10-pin header, p=2.0 mm
- CN Location:** See **Figure 4-15**
- CN Pinouts:** See **Table 4-15**

This connector provides RS-232, RS-422 or RS-485 communications. The default mode is set to RS-232. Use BIOS to configure the connectors as RS-422 or RS-485.

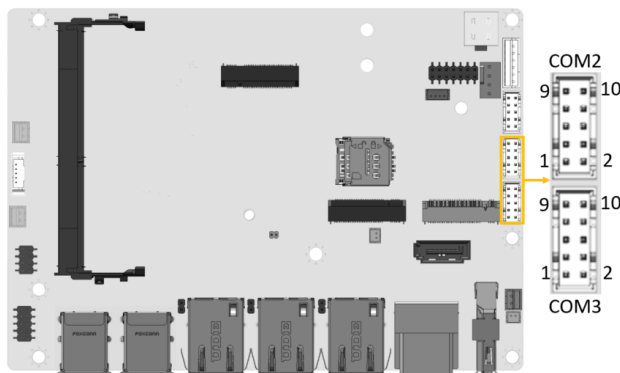


Figure 4-15: RS-232/422/485 Connector Location

| Pin | RS-232 | RS-422 | RS-485 |
|------------|---------------|---------------|---------------|
| 1 | DCD | TXD- | DATA- |
| 2 | DSR | N/A | N/A |
| 3 | RXD | TXD+ | DATA+ |
| 4 | RTS | N/A | N/A |
| 5 | TXD | RXD+ | N/A |
| 6 | CTS | N/A | N/A |
| 7 | DTR | RXD- | N/A |
| 8 | RI | N/A | N/A |
| 9 | GND | N/A | N/A |
| 10 | GND | | |

Table 4-15: RS-232/422/485 Serial Port Connector Pinouts

DRPC-W-TGL

Use the optional RS-232/422/485 cable to connect to a serial device. The pinouts of the DB-9 connector are listed below.

| Pin | RS-232 | RS-422 | RS-485 |
|-----|--------|---------|---------|
| 1 | DCD | TXD422- | TXD485- |
| 2 | RXD | TXD422+ | TXD485+ |
| 3 | TXD | RXD422+ | -- |
| 4 | DTR | RXD422- | -- |
| 5 | GND | -- | -- |
| 6 | DSR | -- | -- |
| 7 | RTS | -- | -- |
| 8 | CTS | -- | -- |
| 9 | RI | -- | -- |

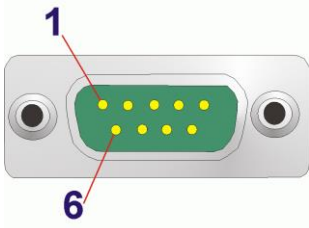


Table 4-16: DB-9 RS-232/422/485 Pinouts

4.2.15 SATA 6Gb/s Drive Connector

- CN Label:** SATA1
- CN Type:** 7-pin SATA connector
- CN Location:** See **Figure 4-16**

The SATA 6Gb/s drive connector is connected to a SATA 6Gb/s drive. The SATA 6Gb/s drive transfers data at speeds as high as 6Gb/s.

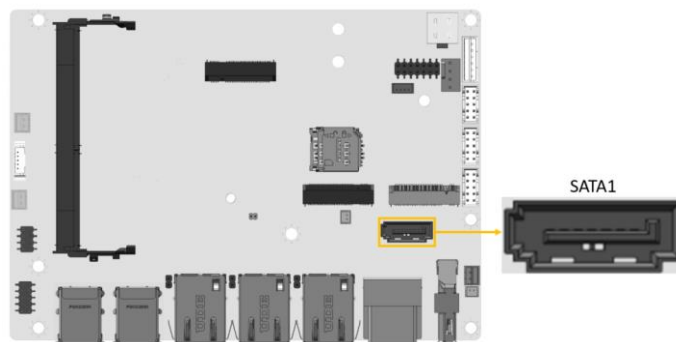


Figure 4-16: SATA 6Gb/s Drive Connectors Location

4.2.16 SATA Power Connector

- CN Label:** SATA_PWR1
- CN Type:** 2-pin wafer, p=2.00 mm
- CN Location:** See **Figure 4-17**
- CN Pinouts:** See **Table 4-17**

The SATA power connector provides +5 V power output to the SATA connector.

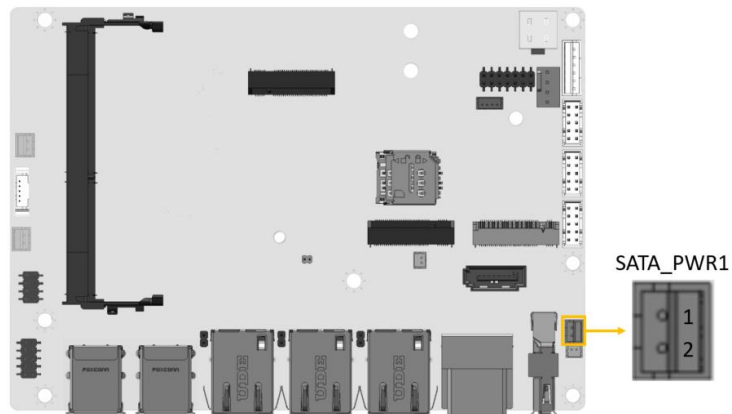


Figure 4-17: SATA Power Connector Location

| Pin | Description |
|-----|-------------|
| 1 | +5V |
| 2 | GND |

Table 4-17: SATA Power Connector Pinouts

DRPC-W-TGL

4.2.17 SMBus/I²C Connector

- CN Label:** I2C1
- CN Type:** 4-pin wafer, p=1.25 mm
- CN Location:** See **Figure 4-18**
- CN Pinouts:** See **Table 4-18**

The SMBus (System Management Bus) connector provides low-speed system management communications.

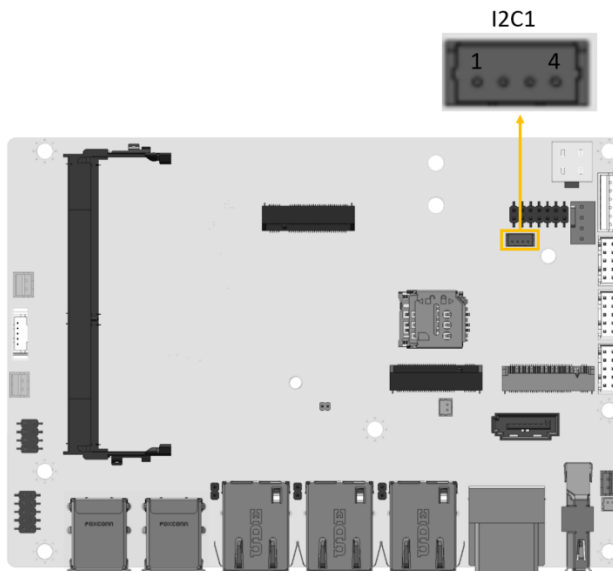


Figure 4-18: SMBus Connector Location

| Pin | Description |
|------------|--------------------|
| 1 | GND |
| 2 | SMBus_DATA |
| 3 | SMBus_CLK |
| 4 | +5V |

Table 4-18: SMBus Connector Pinouts

4.2.18 USB 2.0 Connector

- CN Label:** USB2_CN1
- CN Type:** 8-pin header, p=2.00 mm
- CN Location:** See **Figure 4-19**
- CN Pinouts:** See **Table 4-19**

The USB connector provides two USB 2.0 ports by dual-port USB cable.

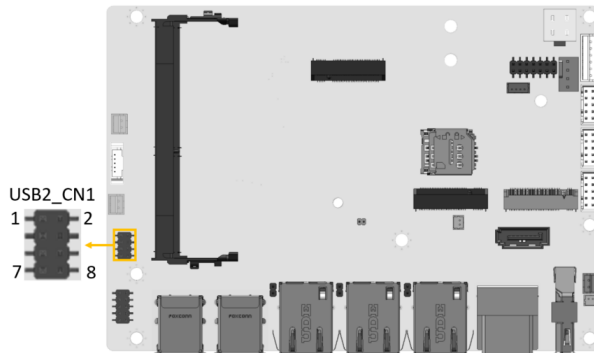


Figure 4-19: USB Connector Location

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|----------------|--------------------|----------------|--------------------|
| 1 | VCC | 2 | GND |
| 3 | DATA- | 4 | DATA+ |
| 5 | DATA+ | 6 | DATA- |
| 7 | GND | 8 | VCC |

Table 4-19: USB Connector Pinouts

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4.3 External Peripheral Interface Connector Panel

Figure 4-20 shows the DRPC-W-TGL Series external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

- 2 x HDMI connector
- 1 x DP connector
- 3 x 2.5GbE RJ-45 connector
- 4 x USB 3.2 Gen 2 connector

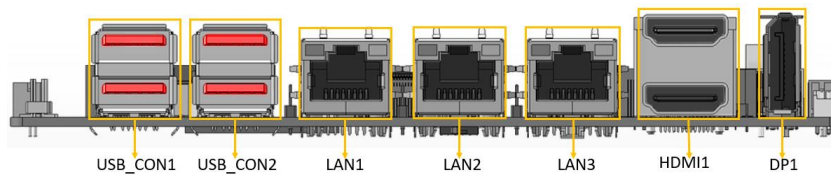


Figure 4-20: External Peripheral Interface Connector

4.3.1 HDMI Connectors

- CN Label:** HDMI1
- CN Type:** HDMI connector
- CN Location:** See **Figure 4-20**
- CN Pinouts:** See **Table 4-20** and **Figure 4-21**

The HDMI connectors can connect to HDMI devices.

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1 | HDMI_DATA2 | 2 | GND |
| 3 | HDMI_DATA2# | 4 | HDMI_DATA1 |
| 5 | GND | 6 | HDMI_DATA1# |
| 7 | HDMI_DATA0 | 8 | GND |
| 9 | HDMI_DATA0# | 10 | HDMI_CLK |
| 11 | GND | 12 | HDMI_CLK# |
| 13 | N/C | 14 | N/C |
| 15 | HDMI_SCL | 16 | HDMI_SDA |
| 17 | GND | 18 | +5V |
| 19 | HDMI_HPD | | |

Table 4-20: HDMI Connector Pinouts

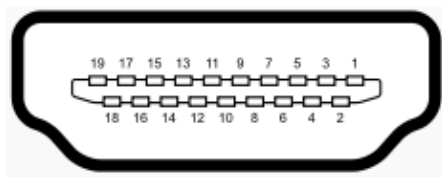


Figure 4-21: HDMI Connector Pinout Locations

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4.3.2 DP Connector

- CN Label:** DP1
- CN Type:** DP connector
- CN Location:** See **Figure 4-20**
- CN Pinouts:** See **Table 4-21** and **Figure 4-22**

The DP connectors can connect to DP devices.

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1 | DATA_0P | 11 | GND |
| 2 | GND | 12 | DATA_3N |
| 3 | DATA_0N | 13 | CONFIG1 |
| 4 | DATA_1P | 14 | CONFIG2 |
| 5 | GND | 15 | AUX_P |
| 6 | DATA_1N | 16 | GND |
| 7 | DATA_2P | 17 | AUX_N |
| 8 | GND | 18 | DP HPD |
| 9 | DATA_2N | 19 | GND |
| 10 | DATA_3P | 20 | DP PWR |

Table 4-21: DP Connector Pinouts

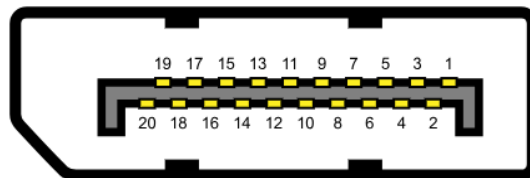


Figure 4-22: DP Connector Pinout Locations

4.3.3 LAN Connectors

- CN Label:** LAN1, LAN2, LAN3
- CN Type:** RJ-45
- CN Location:** See **Figure 4-20**
- CN Pinouts:** See **Figure 4-23** and **Table 4-22**

The LAN connector connects to a local network.

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1 | MDIA0+ | 5 | MDIA2+ |
| 2 | MDIA0- | 6 | MDIA1- |
| 3 | MDIA1+ | 7 | MDIA3+ |
| 4 | MDIA2- | 8 | MDIA3- |

Table 4-22: LAN Pinouts

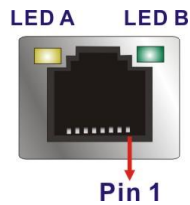


Figure 4-23: LAN Connector

| Activity/Link LED | | Speed LED | |
|-------------------|----------------|-----------|----------------------|
| STATUS | DESCRIPTION | STATUS | DESCRIPTION |
| Off | No link | Off | 10 Mbps connection |
| Yellow | Linked | Green | 1000 Mbps connection |
| Blinking | TX/RX activity | Orange | 2.5 Gbps connection |

Table 4-23: RJ-45 Ethernet Connector LEDs

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4.3.4 USB 3.2 Gen 2 Connectors

- CN Label:** USB_CON1, USB_CON2
- CN Type:** USB 3.2 Gen 2 port
- CN Location:** See **Figure 4-20**
- CN Pinouts:** See **Table 4-24** and **Figure 4-24**

The DRPC-W-TGL Series has four external USB 3.2 Gen 2 ports. The USB connector can be connected to a USB 2.0 or USB 3.2 device. The pinouts of USB 3.2 Gen 2 connectors are shown below.

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1 | VCC | 10 | VCC |
| 2 | USB_DATA0- | 11 | USB_DATA1- |
| 3 | USB_DATA0+ | 12 | USB_DATA1+ |
| 4 | GND | 13 | GND |
| 5 | USB3_RX0- | 14 | USB3_RX1- |
| 6 | USB3_RX0+ | 15 | USB3_RX1+ |
| 7 | GND | 16 | GND |
| 8 | USB3_TX0- | 17 | USB3_TX1- |
| 9 | USB3_TX0+ | 18 | USB3_TX1+ |

Table 4-24: USB 3.2 Gen 2 Port Pinouts

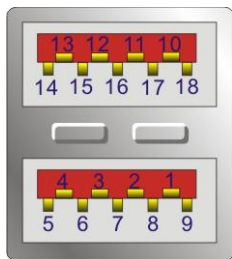
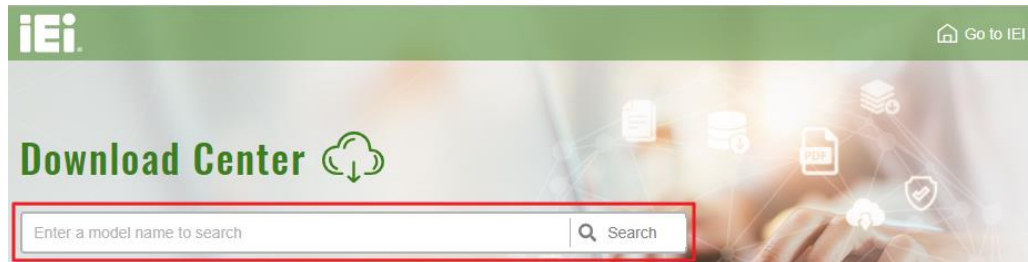


Figure 4-24: USB 3.2 Gen 2 Port Pinouts

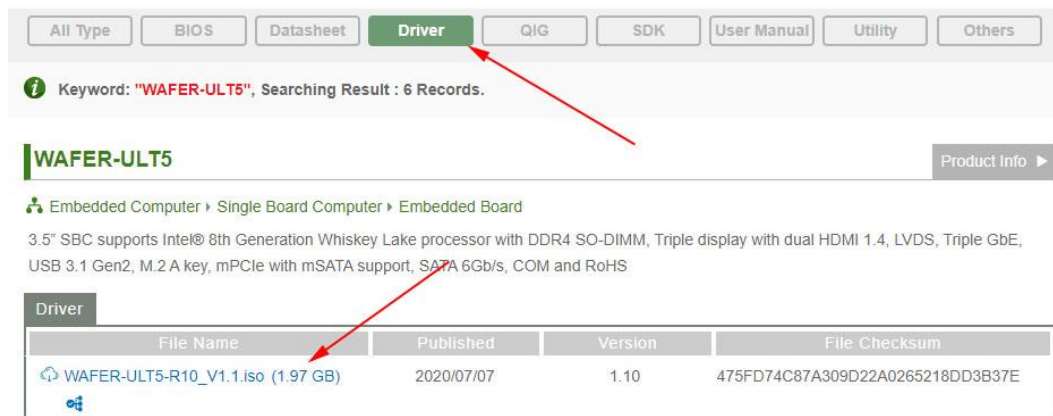
4.4 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

Step 4: Go to <https://download.ieiworld.com>. Type DRPC-W-TGL Series and press Enter.

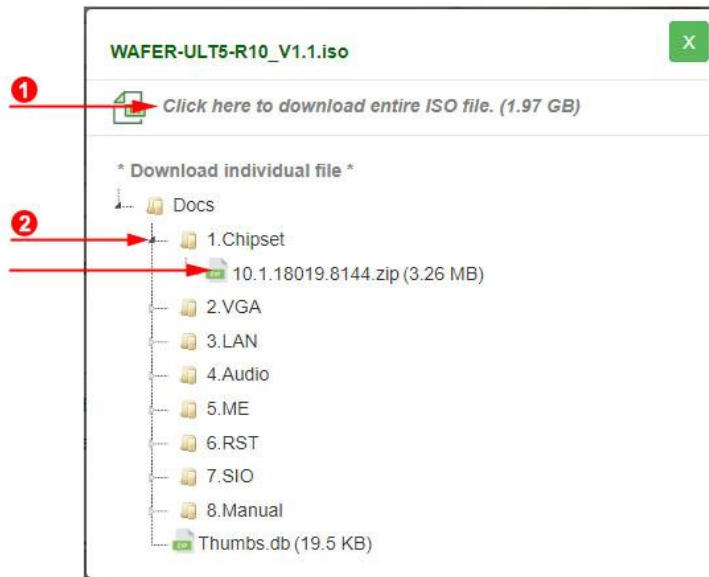


Step 5: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 6: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).

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NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content.

4.5 Available Drivers

All the drivers for the DRPC-W-TGL Series are available on IEI Resource Download Center (<https://download.ieiworld.com>). Type DRPC-W-TGL Series and press Enter to find all the relevant software, utilities, and documentation.

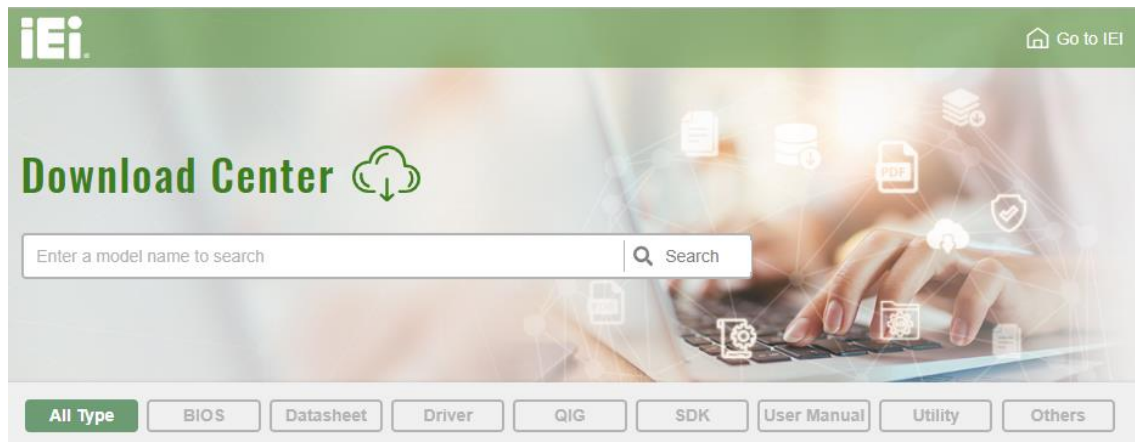


Figure 4-25: IEI Resource Download Center

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.



NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. **Using keyboard:** Press the **DEL** or **F2** as soon as the system is turned on.
2. **Using touchscreen:** Press the **Setup** button on the upper right corner of the BIOS Starting Menu.

If the message disappears before the **DEL** or **F2** key is pressed, restart the computer and try again, then the BIOS Starting Menu will appear. Select "Setup" and press Enter to get into the BIOS Setup.

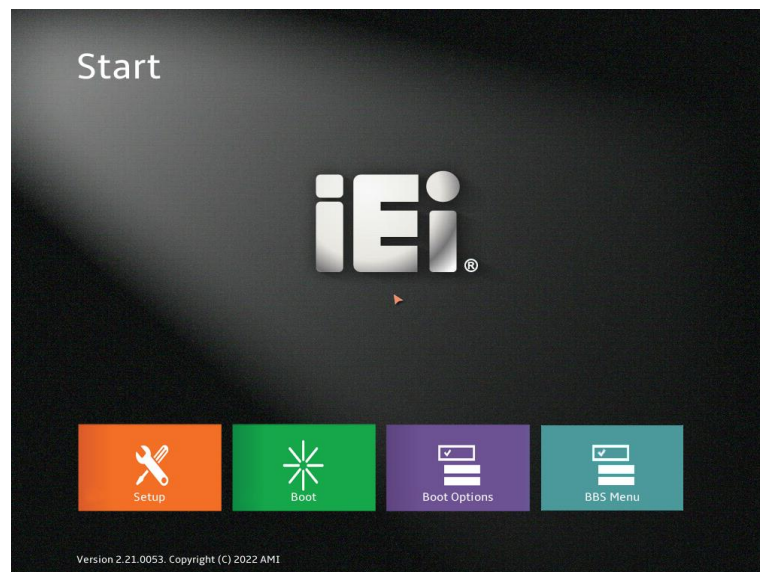


Figure 5-1: BIOS Starting Menu

5.1.2 Using Setup

The BIOS Setup menu can be navigated by using a keyboard or a touchscreen.

5.1.2.1 Keyboard Navigation

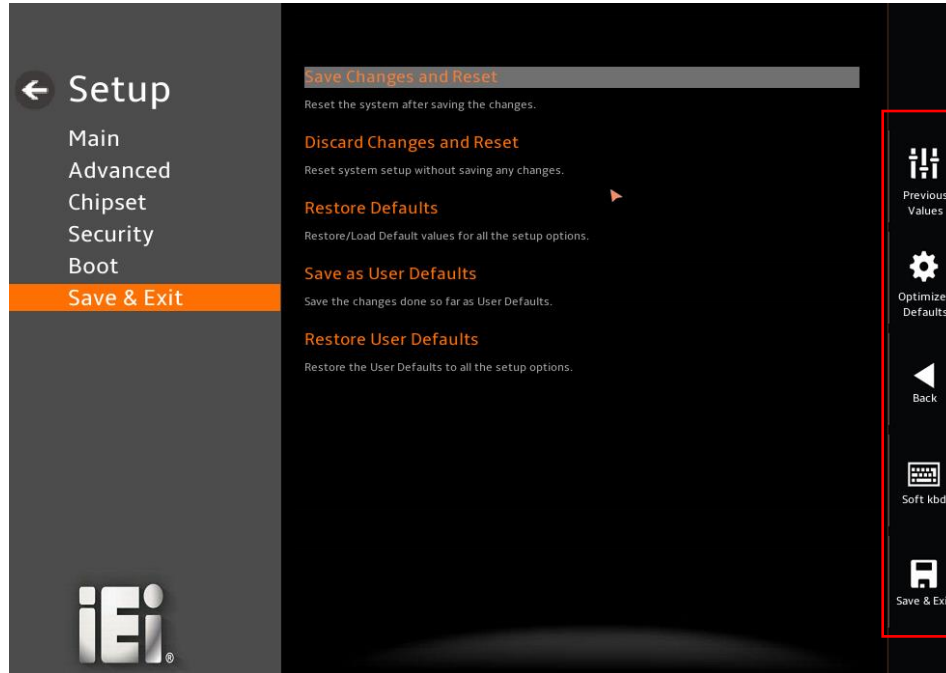
For keyboard navigation, use the navigation keys shown in Table 5-1

| Key | Function |
|-------------|--|
| Up arrow | Move to previous item |
| Down arrow | Move to next item |
| Left arrow | Move to the item on the left hand side |
| Right arrow | Move to the item on the right hand side |
| + | Increase the numeric value or make changes |
| - | Decrease the numeric value or make changes |
| Page Up | Move to the previous page |
| Page Dn | Move to the next page |
| Esc | Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu |
| F1 | General help, only for Status Page Setup Menu and Option Page Setup Menu |
| F2 | Load previous values |
| F3 | Load optimized defaults |
| F4 | Save changes and Exit BIOS |
| <K> | Scroll help area upwards |
| <M> | Scroll help area downwards |

Table 5-1: BIOS Navigation Keys

5.1.2.2 Touch Navigation

For touchscreen navigation, use the on-screen navigation keys shown below.



| On-screen Button | Function |
|--------------------|---|
| Previous Values | Load the last value you set. |
| Optimized Defaults | Load the factory default values in order to achieve the best performance. |
| Back | Return to the previous menu. |
| Soft kbd | Display the on-screen keyboard. |
| Save & Exit | Save the changes made to the BIOS options and reset the system. |

Figure 5-2: BIOS On-screen Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press the **Esc** key.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

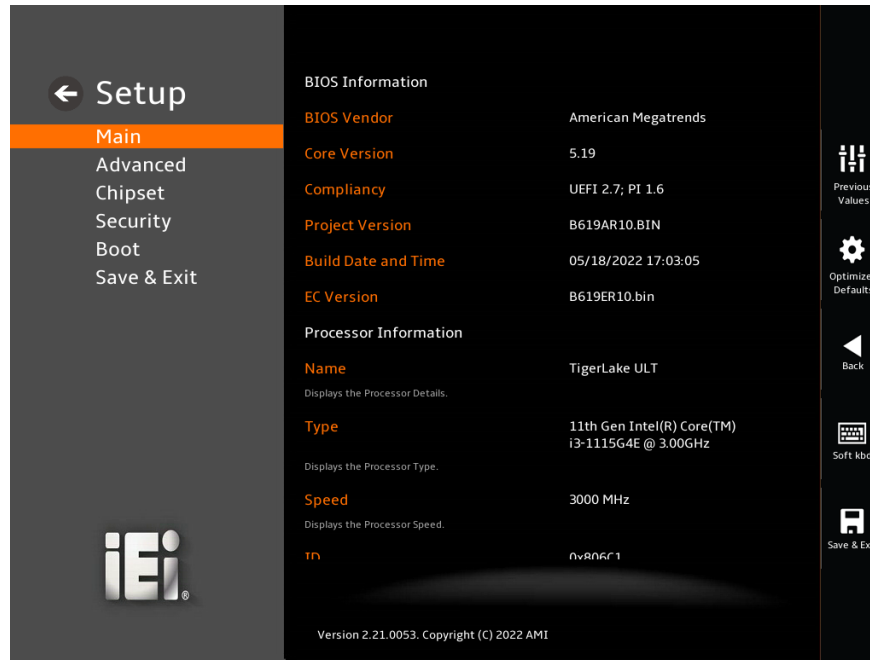
The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

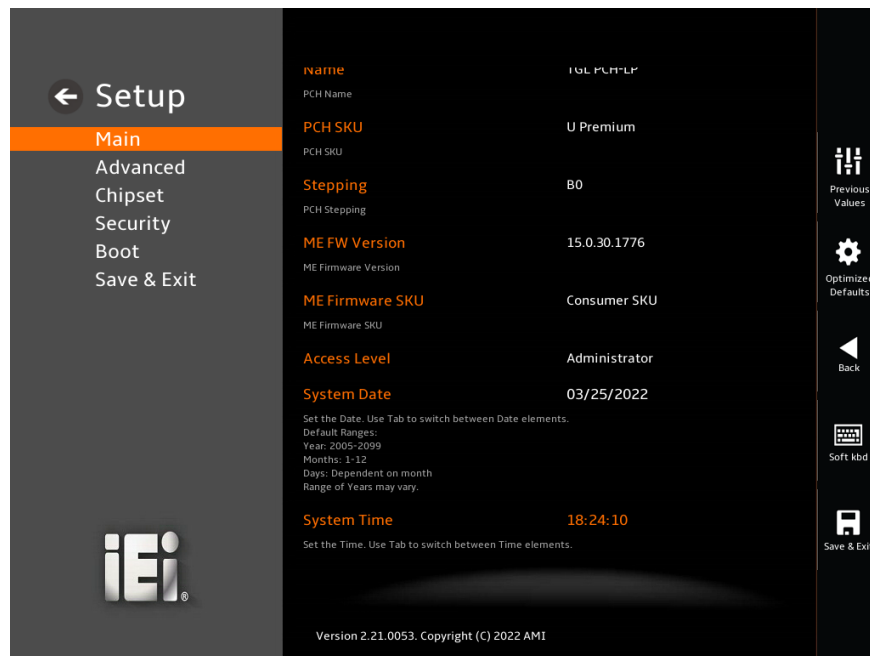
The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1 & BIOS Menu 2**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main (1/2)



BIOS Menu 2: Main (2/2)

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→ BIOS Information

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Compliance:** Current UEFI & PI version
- **Project Version:** the board version
- **Build Date:** Date the current BIOS version was made
- **EC Version:** Current EC version
- BIOS Information

→ Processor Information

The **Processor Information** lists a brief summary of the Processor. The fields in **Processor Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the Processor Details
- **Type:** Displays the Processor Type
- **Speed:** Displays the Processor Speed
- **ID:** Displays the Processor ID
- **Stepping:** Displays the Processor Stepping
- **Package:** Displays the Processor Package
- **Number of Processors:** Displays number of CPU cores
- **Microcode Revision:** CPU Microcode Revision
- **GT Info:** Processor GT Info. Only valid if SNB stepping is D0 or above
- **IGFX GOP Version:** Displays the IGFX GOP Version
- **PCIe GEN4 Dekel FW Version:** Dekel Firmware Version used by PCIe Gen4 PHY
- **SAM Firmware Version:** System Agent Manage ability Engine FW Version
- **Memory RC Version:** Displays the Memory RC Version
- **Total Memory:** Total Memory in the System
- **Memory Frequency:** Displays the Frequency of Memory

→ PCH Information

The **PCH Information** lists a brief summary of the PCH. The fields in **PCH Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the PCH Name
- **PCH SKU:** Displays the PCH SKU
- **Stepping:** Displays the PCH Stepping
- **Dual Output Fast Read support:** Displays the Processor Details
- **Read ID/Status Clock Freq:** Displays the Read ID and Read Status Clock Frequency
- **Write and Erase Clock Freq:** Displays the Write and Erase Clock Frequency
- **ME FW Version:** Displays the ME Firmware Version
- **ME Firmware SKU:** Displays the ME Firmware SKU
- **PMC FW Version:** Displays the PMC Firmware Version

The System Overview field also has two user configurable fields:

→ System Date [xx/xx/xx]

Use the **System Date** option to set the system date. Manually enter the day, month and year.

→ System Time [xx:xx:xx]

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

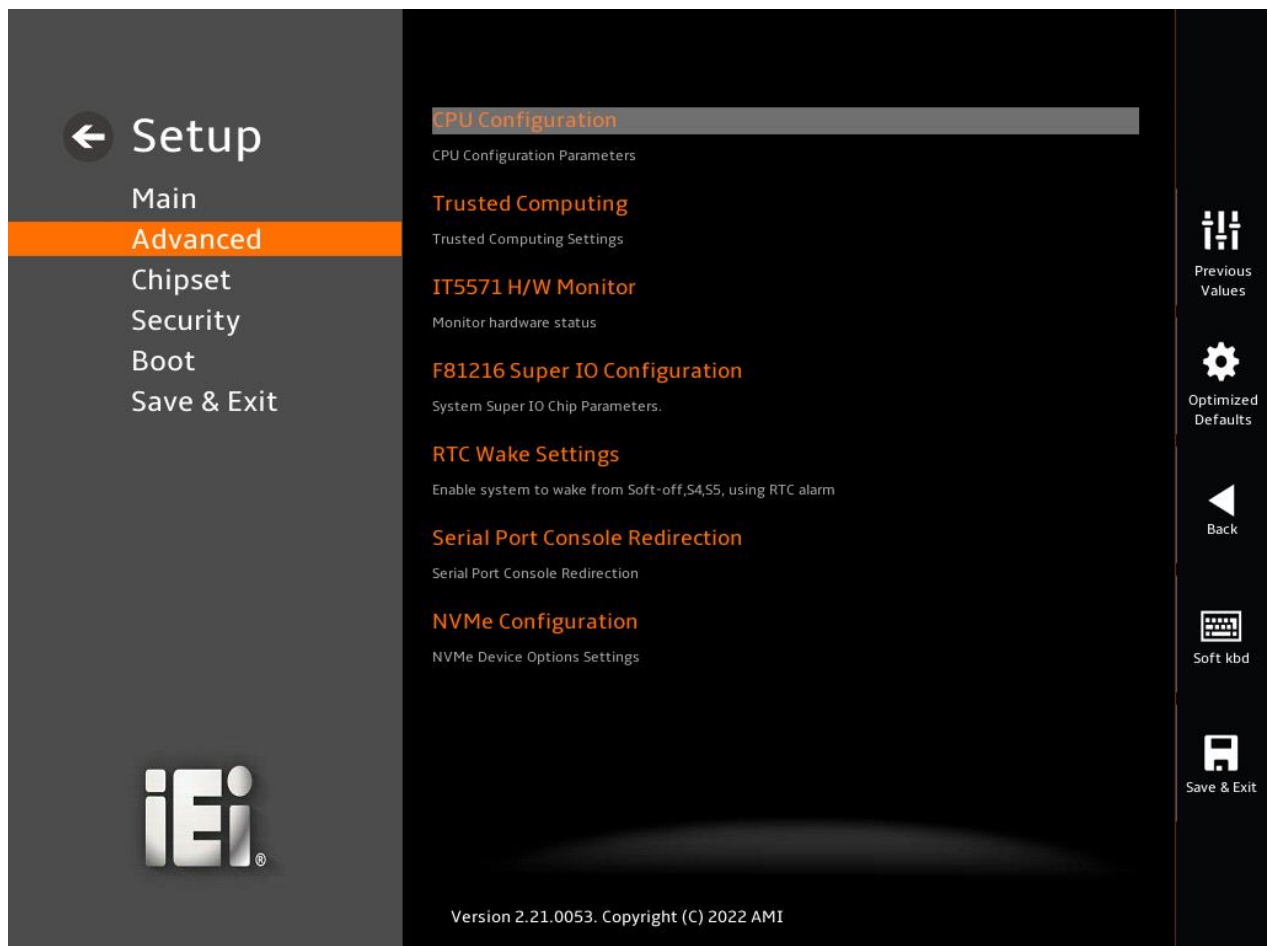
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5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 3**) to configure the CPU and peripheral devices through the following sub-menus:

**WARNING!**

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.



BIOS Menu 3: Advanced

5.3.1 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 4 & BIOS Menu 5 & BIOS Menu 6**) to view detailed CPU specifications or enable the Intel Virtualization Technology.



BIOS Menu 4: CPU Configuration (1/3)

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Setup

- Main
- Advanced**
- Chipset
- Security
- Boot
- Save & Exit

Power Limit 1

Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU. Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs; This value must be between Min Power Limit and TDP Limit.

Turbo Mode

Enable/Disable processor Turbo Mode (requires EMTM enabled too). AUTO means enabled.

Power Limit 1 Time Window

Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.

Power Limit 2

Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.

Intel (VMX) Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

Number of cores to enable in each processor package.

Hyper-Threading

Enable or Disable Hyper-Threading Technology.

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Navigation icons: Previous Values, Optimized Defaults, Back, Soft kbd, Save & Exit

BIOS Menu 5: CPU Configuration (2/3)

Setup

- Main
- Advanced**
- Chipset
- Security
- Boot
- Save & Exit

Power Limit 1 Time Window

Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.

Power Limit 2

Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.

Intel (VMX) Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

Number of cores to enable in each processor package.

Hyper-Threading

Enable or Disable Hyper-Threading Technology.

EIST

Allows more than two frequency ranges to be supported.

C states

Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.

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Navigation icons: Previous Values, Optimized Defaults, Back, Soft kbd, Save & Exit

BIOS Menu 6: CPU Configuration (3/3)

→ Power Limit 1 [0]

Use the + or – key to change the **Power Limit 1** value. BIOS will program the default values for Limit 1 and Power Limit 1 Time Window. For 12.50W, enter 12500.

→ Power Limit 2 [0]

Use the + or – key to change the **Power Limit 2** value. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500.

→ Power Limit 1 Time Window [0]

Use the **Power Limit 1 Time Window** option to select the PL1 time duration. The value may vary from 0 to 128. For 0 is the default value

→ Turbo Mode [Enabled]

Use the **Turbo Mode** option to enable or disable Turbo Mode which requires Intel Speed Step or Intel Speed Shift to be available and enabled.

- Disabled** Disables Turbo Mode Technology
- Enabled** **DEFAULT** Enables Turbo Mode Technology

→ Intel (VMX) Virtualization Technology [Disabled]

Use the **Intel (VMX) Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

- Disabled** Disables Intel Virtualization Technology.
- Enabled** **DEFAULT** Enables Intel Virtualization Technology.

→ Active Processor Cores [All]

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

- All** **DEFAULT** Enable all cores in the processor package.

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- 1 Enable one core in the processor package.
- 2 Enable two cores in the processor package.
- 3 Enable three cores in the processor package.

→ Hyper-Threading [Enabled]

Use the **Hyper-Threading** option to enable or disable the **Hyper-Threading** Technology.

- **Disabled** Disables Hyper-Threading Technology
- **Enabled** **DEFAULT** Enables Hyper-Threading Technology

→ EIST [Enabled]

Use the **EIST** option to enable or disable the capability that allows more than two frequency ranges to be supported.

- **Disabled** Disables the EIST Technology
- **Enabled** **DEFAULT** Enables the EIST Technology

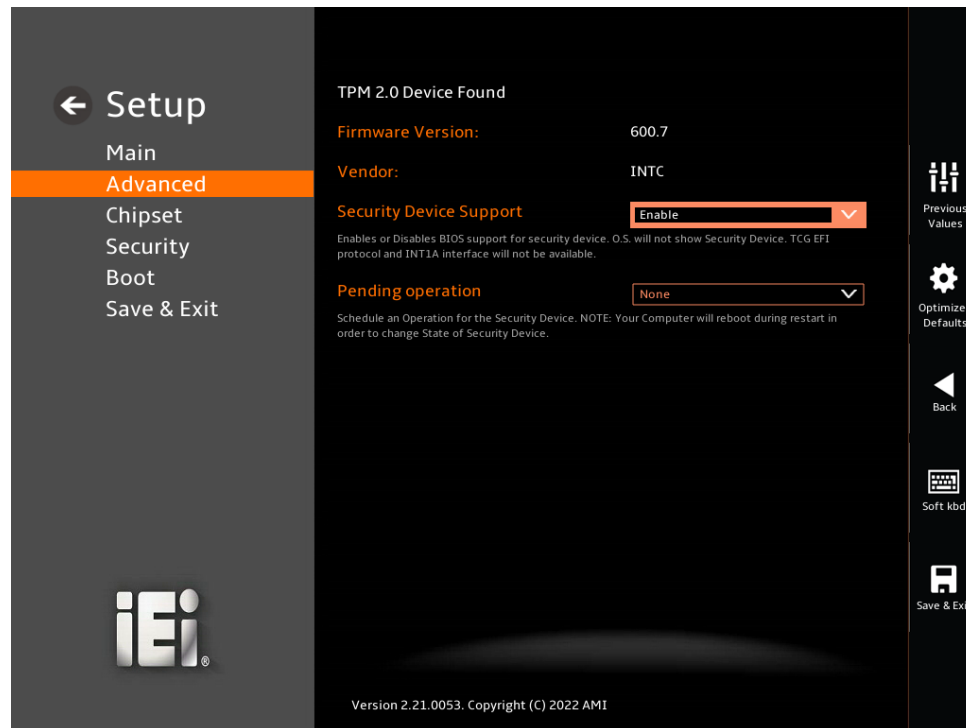
→ C states [Disabled]

Use the **C states** option to enable or disable CPU power management which allows CPU to go to C states when it is not 100% utilized.

- **Disabled** **DEFAULT** Disables CPU power management
- **Enabled** Enables CPU power management

5.3.2 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 7**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).



BIOS Menu 7: PCH-FW Configuration

→ Security Device Support [Enable]

Use the **Security Device Support** option to configure support for the TPM.

- **Disable** TPM support is disabled.
- **Enable** **DEFAULT** TPM support is enabled.

→ Pending Operation [None]

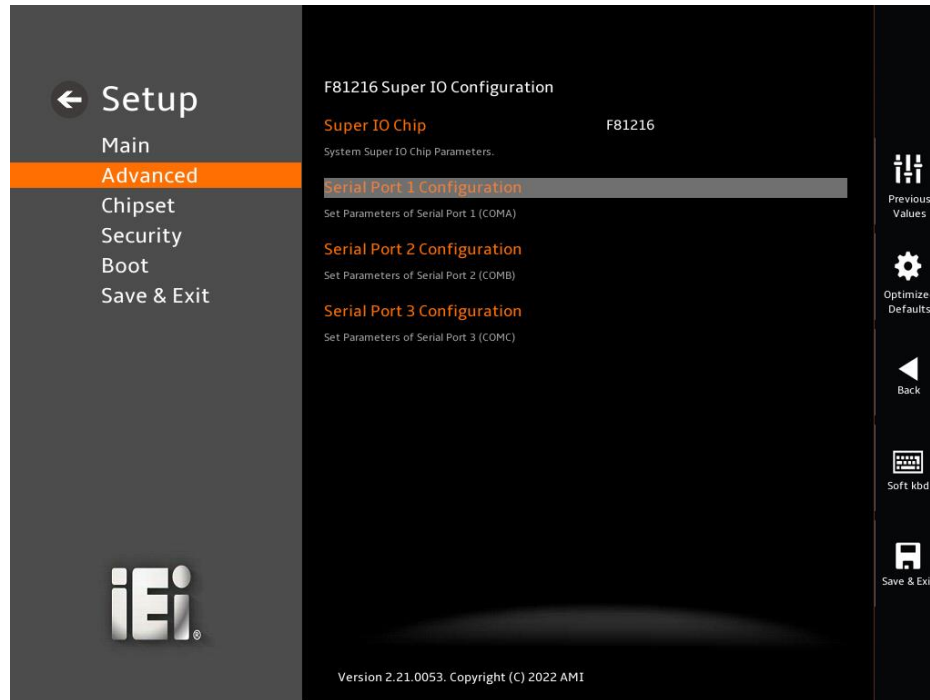
Use the **Pending Operation** option to schedule an operation for the security device.

- **None** **DEFAULT** TPM information is previous.S
- **TPM Clear** TPM information is cleared

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5.3.3 F81216 Super IO Configuration

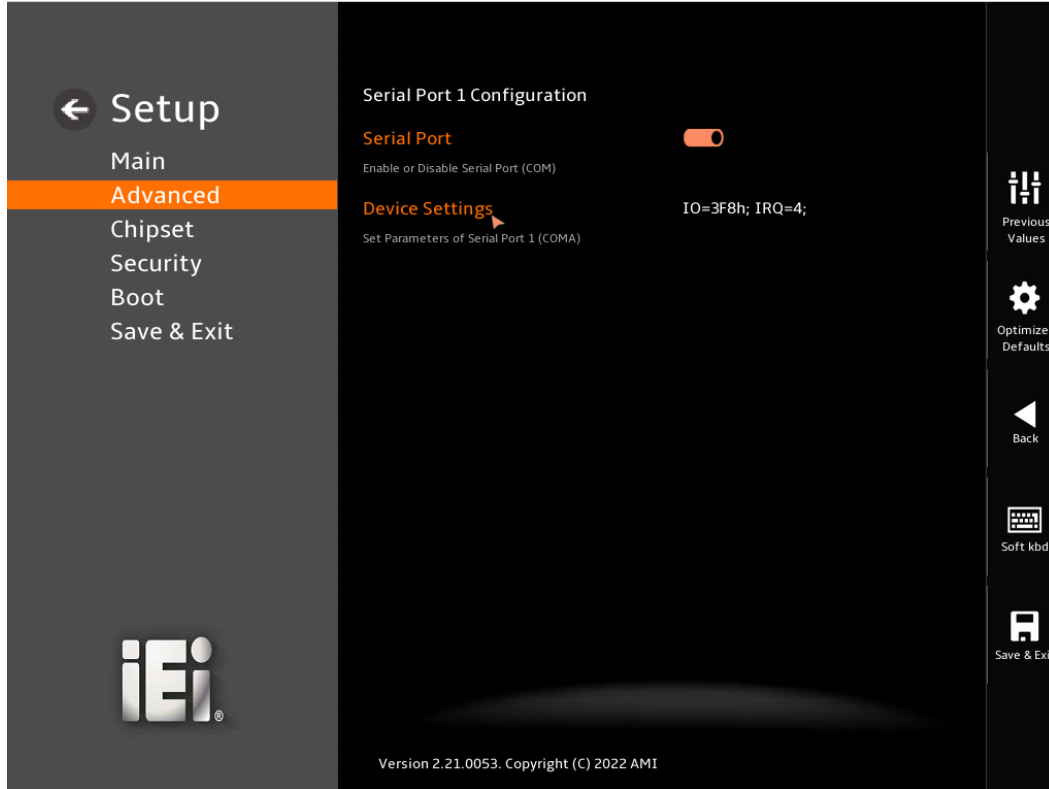
Use the **F81216 Super IO Configuration** menu (**BIOS Menu 8**) to set or change the configurations for the serial ports.



BIOS Menu 8: F81966 Super IO Configuration

5.3.3.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 9**) to configure the serial port n.



BIOS Menu 9: Serial Port 1 Configuration Menu

➔ Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port
- ➔ **Enabled DEFAULT** Enable the serial port

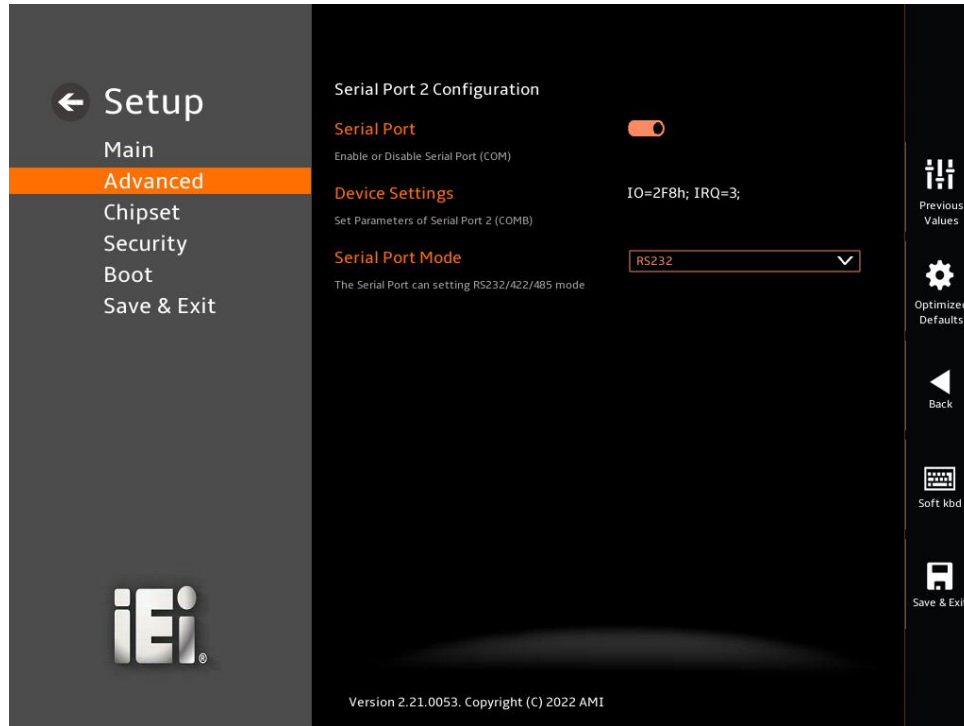
➔ Device Settings

The **Device Settings** option shows the serial port IO port address and interrupt address.

- ➔ **IO=3F8h;** Serial Port I/O port address is 3F8h and the interrupt
IRQ=4 address is IRQ4

5.3.3.2 Serial Port 2 Configuration

Use the **Serial Port 2 Configuration** menu (**BIOS Menu 10**) to configure the serial port.



BIOS Menu 10: Serial Port 2 Configuration Menu

→ Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- **Disabled** Disable the serial port
- **Enabled** **DEFAULT** Enable the serial port

→ Device Settings

The **Device Settings** option shows the serial port IO port address and interrupt address.

- **IO=2F8h;** Serial Port I/O port address is 2F8h and the interrupt
IRQ=3 address is IRQ3

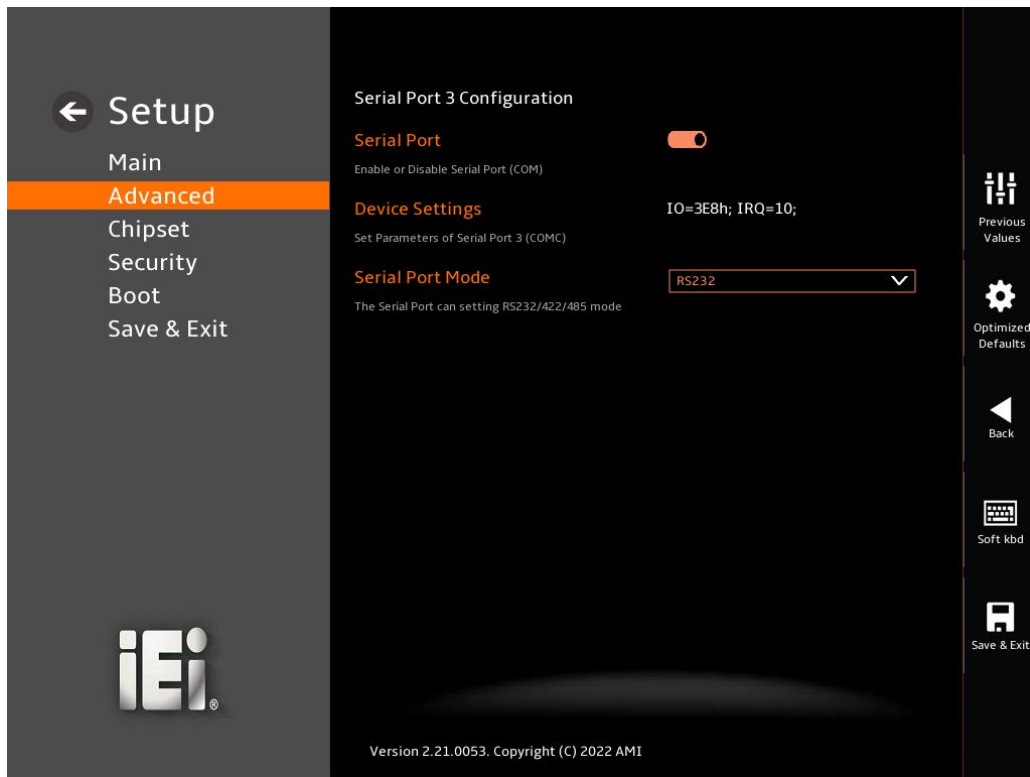
➔ **Serial Port Mode [RS232]**

Use the **Serial Port Mode** option to set RS232/422/485 mode.

- ➔ **RS232** Serial Port Mode is RS232 mode
- ➔ **RS422** Serial Port Mode is RS422 mode
- ➔ **RS485** Serial Port Mode is RS485 mode

5.3.3.3 Serial Port 3 Configuration

Use the **Serial Port 3 Configuration** menu (**BIOS Menu 11**) to configure the serial port 3.



BIOS Menu 11: Serial Port 3 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port

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➔ **Enabled** **DEFAULT** Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2E0h;** Serial Port I/O port address is 2E0h and the interrupt
IRQ=10 address is IRQ10

➔ **Serial Port Mode [RS232]**

Use the **Serial Port Mode** option to set RS232/422/485 mode.

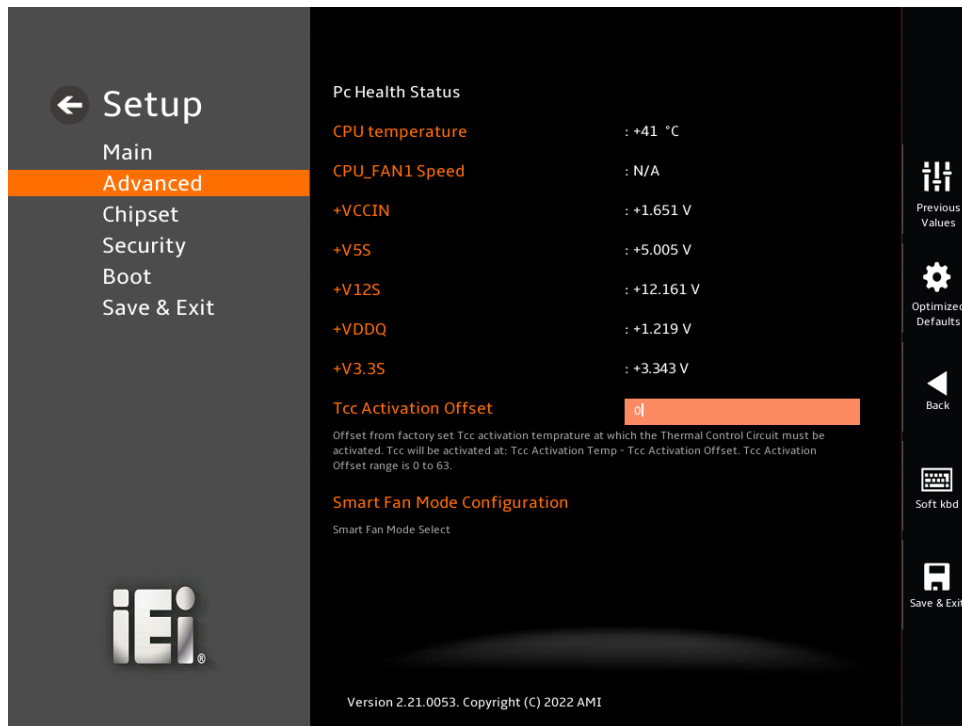
➔ **RS232** Serial Port Mode is RS232 mode

➔ **RS422** Serial Port Mode is RS422 mode

➔ **RS485** Serial Port Mode is RS485 mode

5.3.4 IT5571 H/W Monitor

The IT5571 H/W Monitor menu (**BIOS Menu 12**) contains the smart fan mode configuration submenu and shows the state of H/W real-time operating temperature, fan speeds and system voltages.



BIOS Menu 12: IT5571 H/W Monitor

→ PC Health Status

The following system parameters and values are shown. The system parameters that are monitored are:

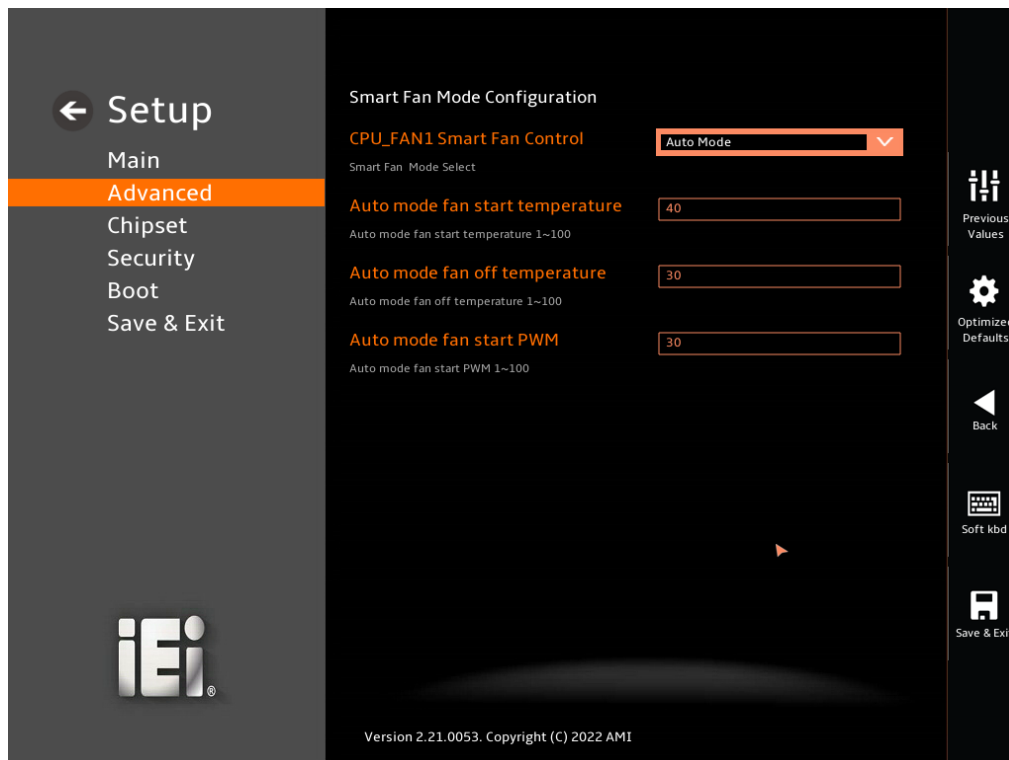
- System Temperatures:
 - CPU Temperature
- Fan Speeds:
 - CPU Fan Speed
- Voltages:
 - +VCCIN

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- +V5S
- +V12S
- +VDDQ
- +V3.3S

5.3.4.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 13**) to configure the CPU/system fan start/off temperature and control mode.



BIOS Menu 13: Smart Fan Mode Configuration

→ CPU_FAN1 Smart Fan Control [Auto Mode]

Use the **CPU_FAN1 Smart Fan Control** option to configure the CPU Smart Fan.

→ Manual Mode

The fan spins at the speed set in Manual Mode settings.

→ **Auto Mode** **DEFAULT** The fan adjusts its speed using Auto Mode settings.

→ **CPU_FAN1 Start Temperature**

If the CPU temperature is between **fan off** and **fan start**, the fan speed change to **fan start PWM**. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

→ **CPU_FAN1 Off Temperature**

If the CPU temperature is lower than the value set this option, the fan speed change to be lowest. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

→ **CPU_FAN1 Start PWM**

Use the **CPU_FAN1 Start PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.

→ **SYS_FAN1 Smart Fan Control [Auto Mode]**

Use the **SYS_FAN1 Smart Fan Control** option to configure the System Smart Fan.

→ **Manual Mode** The fan spins at the speed set in Manual Mode settings.

→ **Auto Mode** **DEFAULT** The fan adjusts its speed using Auto Mode settings.

→ **SYS_FAN1 Start Temperature**

If the System temperature is between **fan off** and **fan start**, the fan speed change to **fan start PWM**. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

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→ SYS_FAN1 Off Temperature

If the System temperature is lower than the value set this option, the fan speed change to be lowest. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

→ SYS_FAN1 Start PWM

Use the **SYS_Fan1 Start PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.

→ Auto Mode Fan Slope PWM

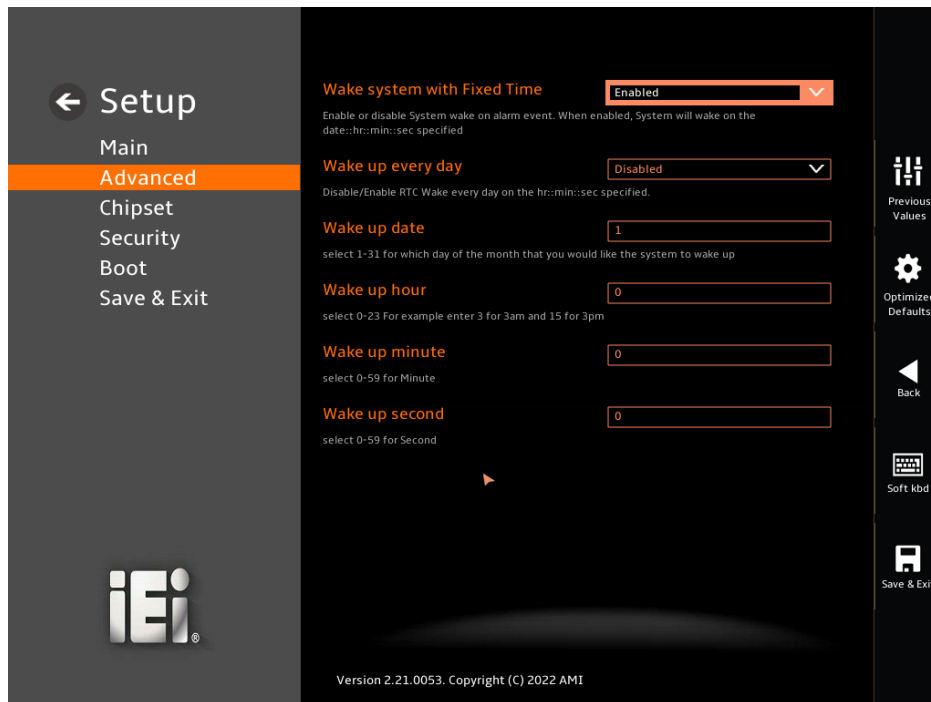
Use the **Auto Mode Fan Slope PWM** option to select the linear rate at which the PWM mode increases with respect to an increase in temperature. Use the + or – key to change the value or enter a decimal number between 1 and 8

5.3.5 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 14**) configures RTC wake event.



BIOS Menu 14: RTC Wake Settings (1/2)



BIOS Menu 15: RTC Wake Settings (2/2)

➔ **Wake system with Fixed Time [Disabled]**

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

➔ **Disabled** **DEFAULT** The real time clock (RTC) cannot generate a wake event

➔ **Enabled** If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected:

Wake up date

Wake up hour

Wake up minute

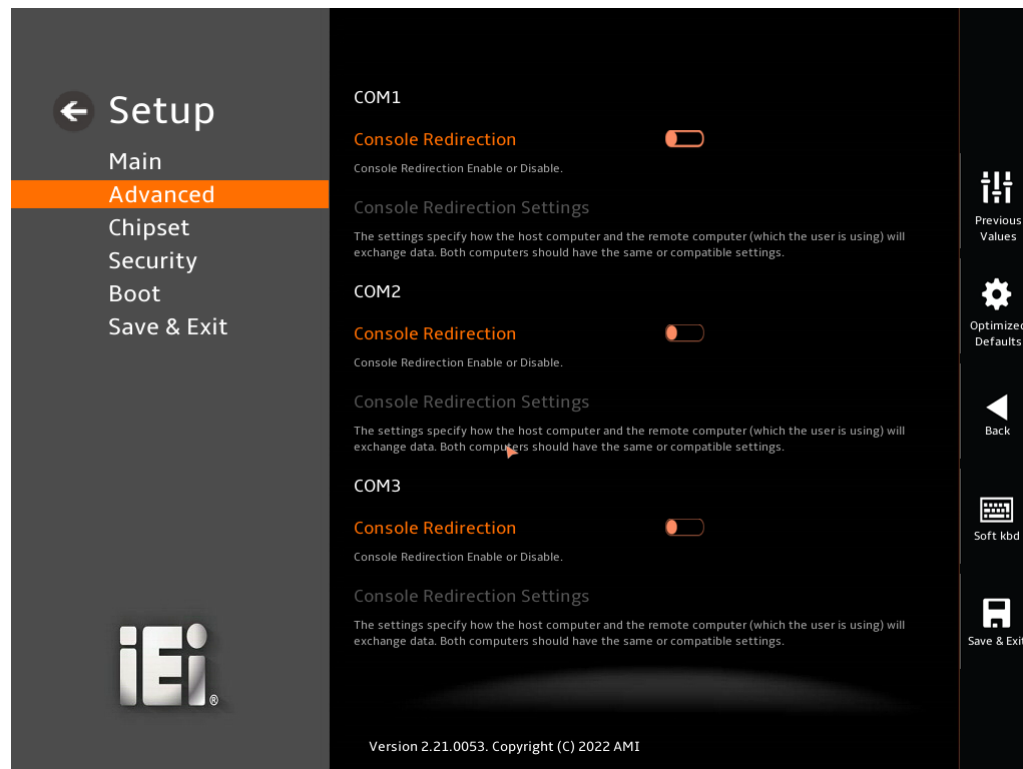
Wake up second

After setting the alarm, the computer turns itself on

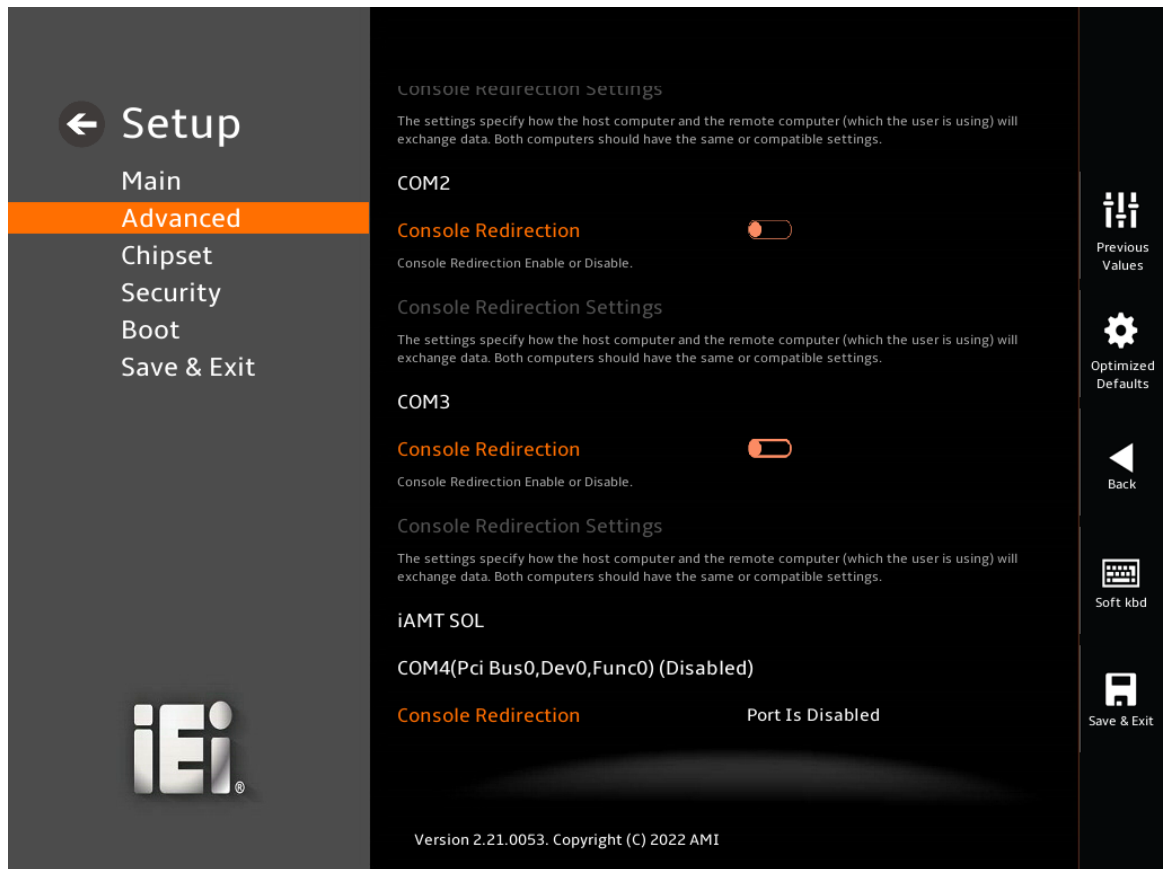
from a suspend state when the alarm goes off.

5.3.6 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 16 & BIOS Menu 17**) allows the console redirection options to be configured. Console Redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 16: Serial Port Console Redirection (1/2)



BIOS Menu 17: Serial Port Console Redirection (2/2)

➔ **Console Redirection [Disabled]**

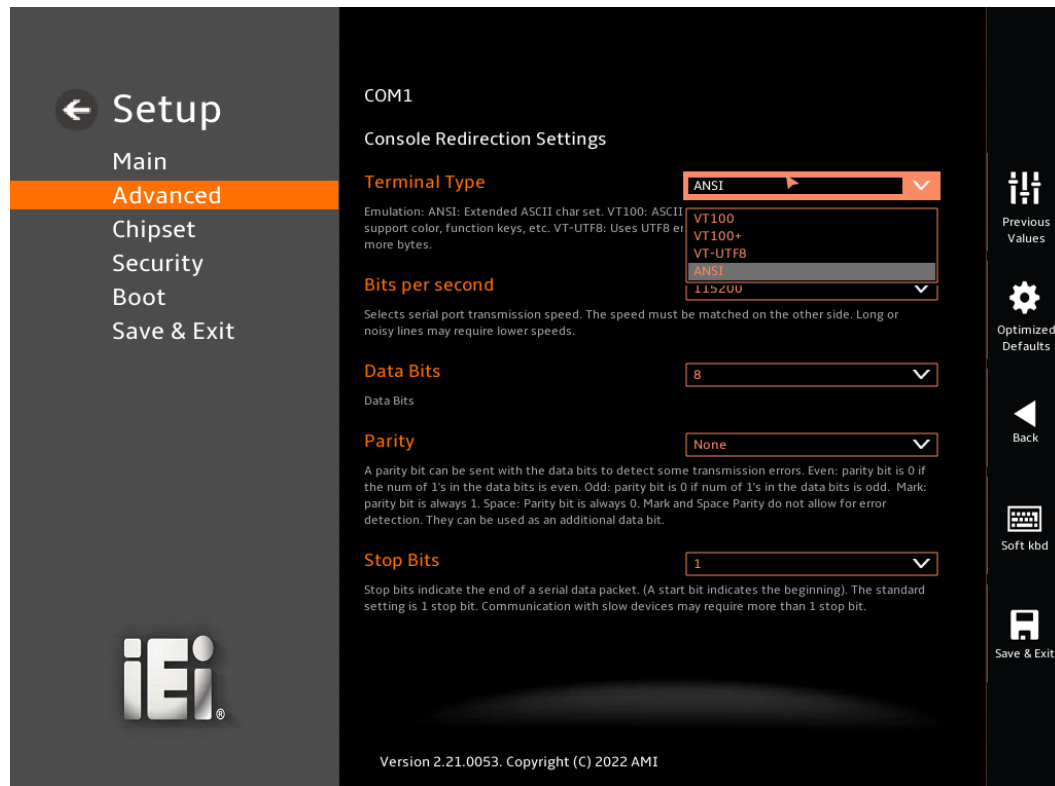
Use **Console Redirection** option to enable or disable the console redirection function.

- ➔ **Disabled** **DEFAULT** Disabled the console redirection function
- ➔ **Enabled** Enabled the console redirection function

The **Console Redirection Settings** submenu will be available when the **Console Redirection** option is enabled.

5.3.6.1 Console Redirection Settings

The following options are available in the **Console Redirection Settings** submenu (**BIOS Menu 18**) when the **COM Console Redirection** (for COM1 to COM6) option is enabled.



BIOS Menu 18: COM Console Redirection Settings

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

- ➔ **VT100** The target terminal type is VT100
- ➔ **VT100+** The target terminal type is VT100+
- ➔ **VT-UTF8** The target terminal type is VT-UTF8
- ➔ **ANSI** **DEFAULT** The target terminal type is ANSI

→ Bits per second [115200]

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match on the other side. Long or noisy lines may require lower speeds.

- | | | |
|-----------------|----------------|--|
| → 9600 | | Sets the serial port transmission speed at 9600. |
| → 19200 | | Sets the serial port transmission speed at 19200. |
| → 38400 | | Sets the serial port transmission speed at 38400. |
| → 57600 | | Sets the serial port transmission speed at 57600. |
| → 115200 | DEFAULT | Sets the serial port transmission speed at 115200. |

→ Data Bits [8]

Use the **Data Bits** option to specify the number of data bits.

- | | | |
|------------|----------------|--------------------------|
| → 7 | | Sets the data bits at 7. |
| → 8 | DEFAULT | Sets the data bits at 8. |

→ Parity [None]

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- | | | |
|----------------|----------------|---|
| → None | DEFAULT | No parity bit is sent with the data bits. |
| → Even | | The parity bit is 0 if the number of ones in the data bits is even. |
| → Odd | | The parity bit is 0 if the number of ones in the data bits is odd. |
| → Mark | | The parity bit is always 1. This option does not allow for error detection. |
| → Space | | The parity bit is always 0. This option does not allow for error detection. |

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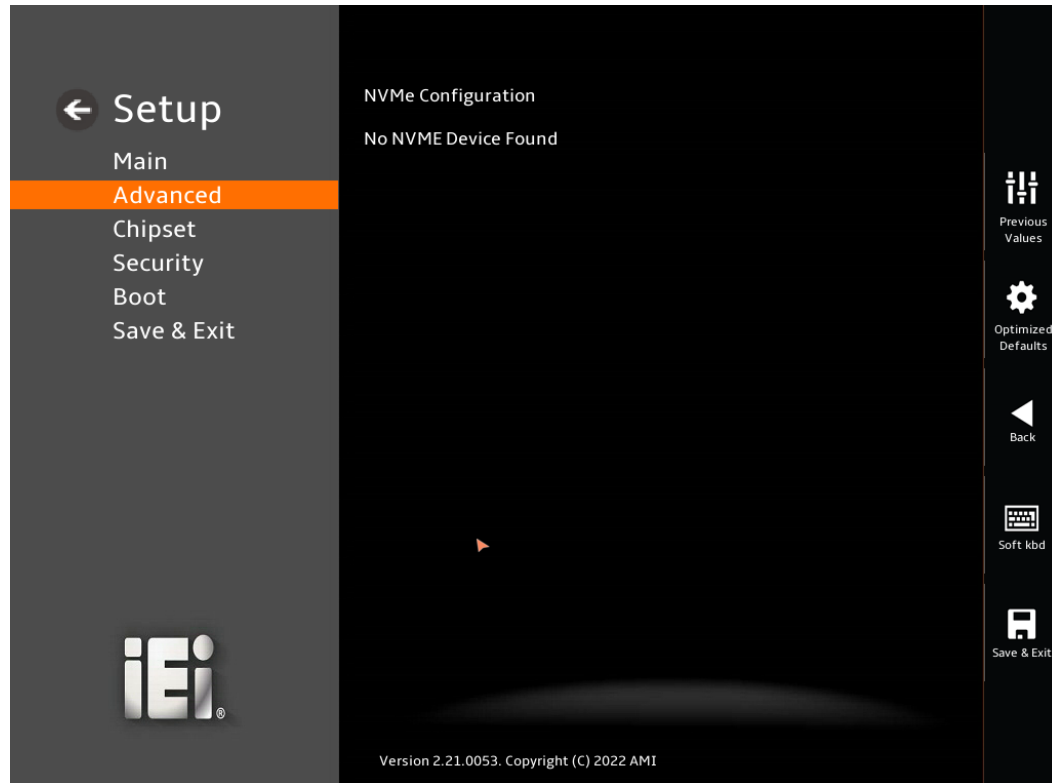
→ Stop Bits [1]

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

- 1 **DEFAULT** Sets the number of stop bits at 1.
- 2 Sets the number of stop bits at 2.

5.3.7 NVMe Configuration

Use the **NVMe Configuration (BIOS Menu 19)** menu to display the NVMe controller and device information.



BIOS Menu 19: NVMe Configuration

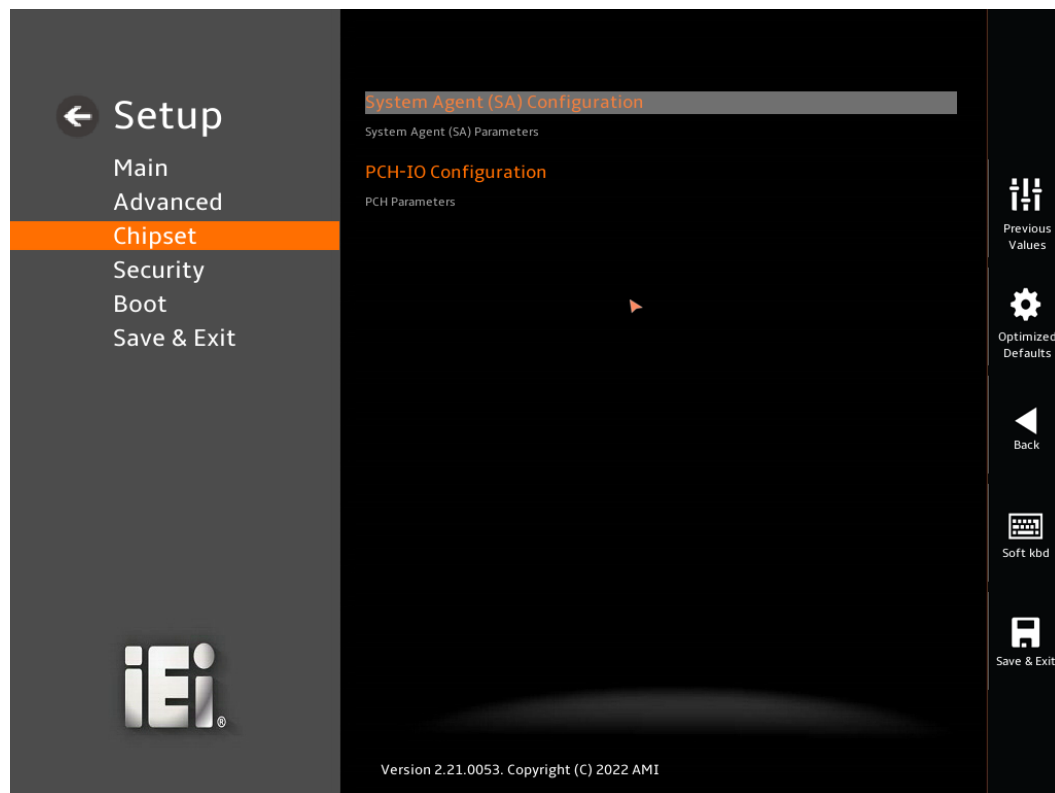
5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 20**) to access the PCH IO and System Agent (SA) configuration menus.



WARNING!

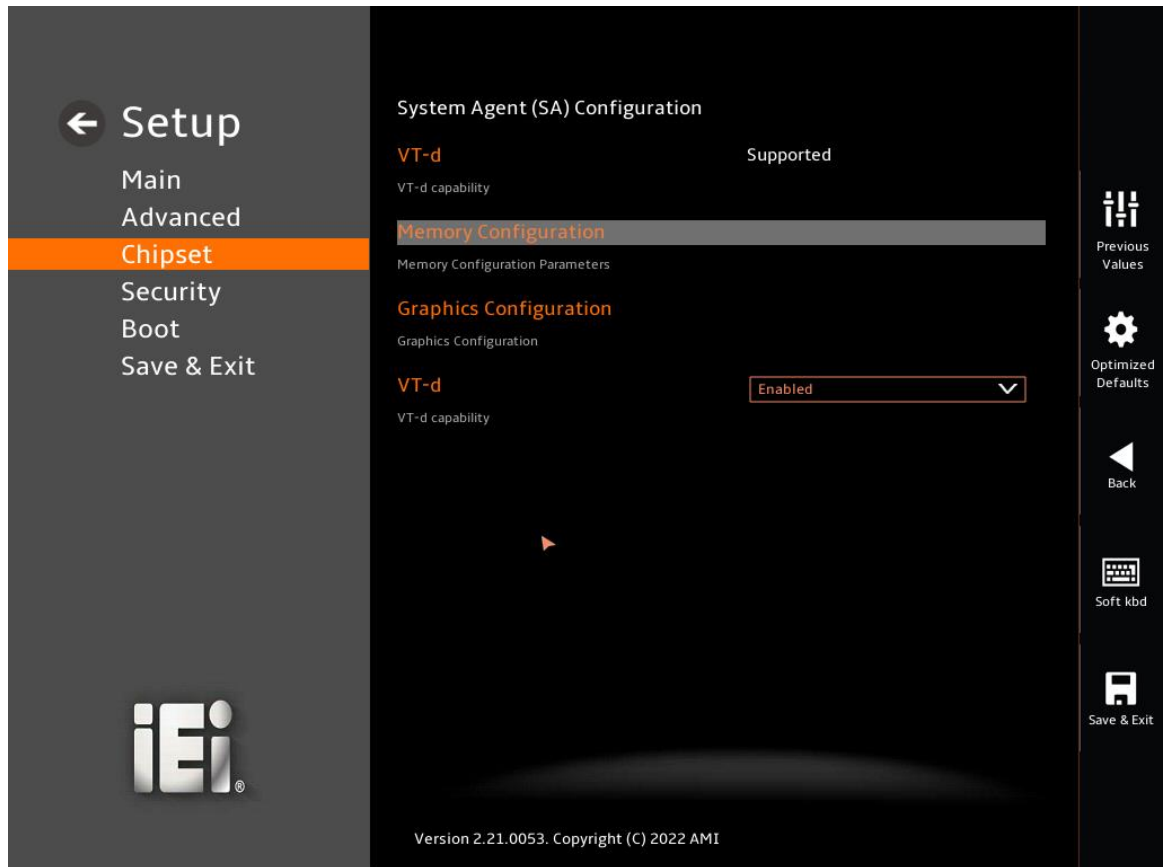
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.



BIOS Menu 20: Chipset

5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 21**) to configure the System Agent (SA) parameters.



BIOS Menu 21: System Agent (SA) Configuration

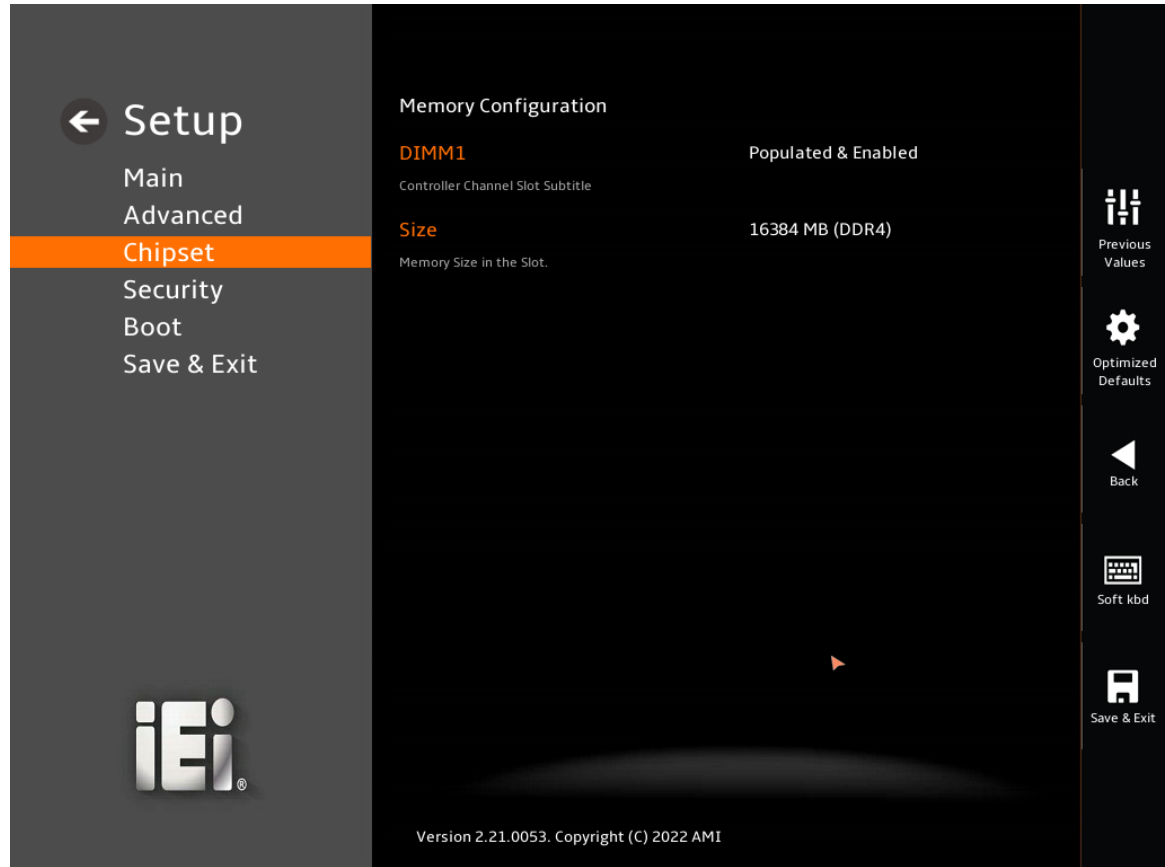
➔ **VT-d [Enabled]**

Use the **VT-d** option to enable or disable the VT-d capability.

- ➔ **Disabled** Disable the VT-d capability
- ➔ **Enabled** **DEFAULT** Enable the VT-d capability

5.4.1.1 Memory Configuration

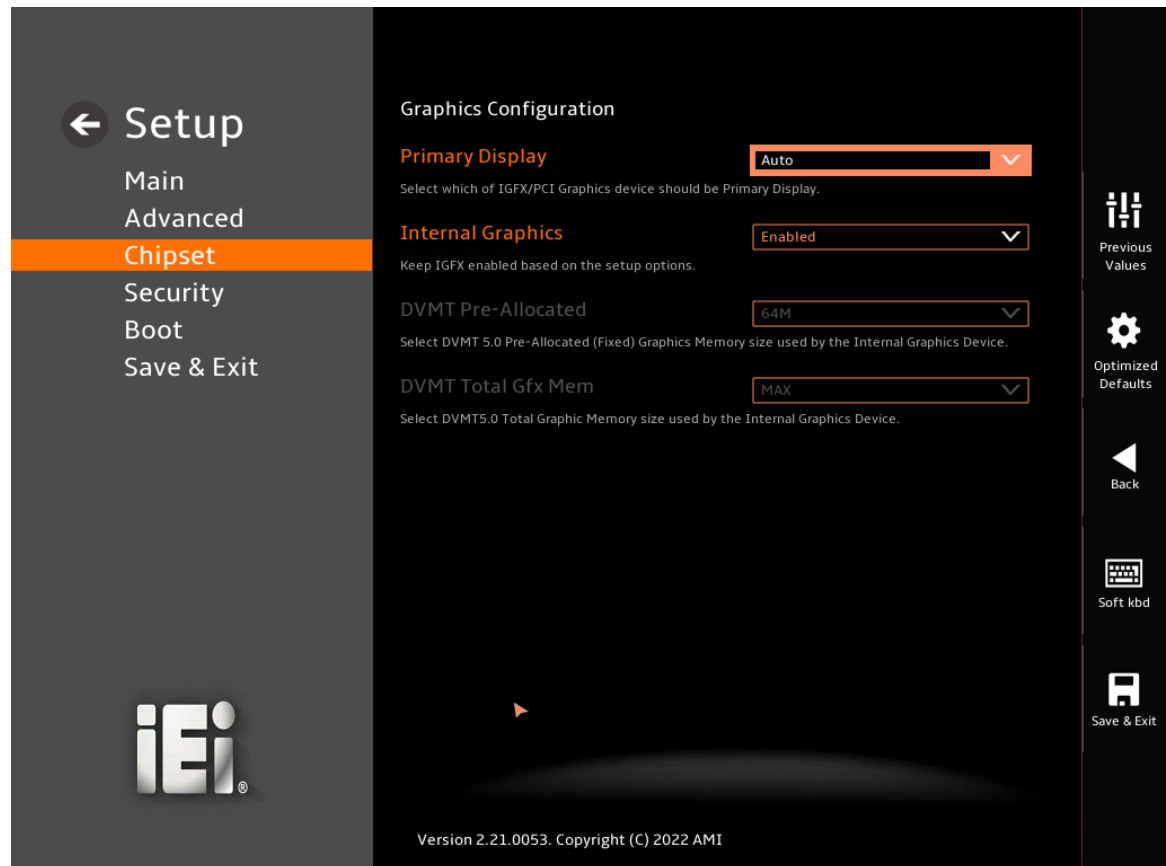
Use the **Memory Configuration** submenu (**BIOS Menu 22**) to view memory information.



BIOS Menu 22: Memory Configuration

5.4.1.2 Graphics Configuration

Use the **Graphics Configuration (BIOS Menu 23)** menu to configure the video device connected to the system.



BIOS Menu 23: Graphics Configuration

→ Primary Display [Auto]

Use the **Primary Display** option to select the primary graphics controller the system uses.

The following options are available:

- Auto **Default**
- IGFX
- PEG
- PCI
- SG

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→ Internal Graphics [Enabled]

Use the **Internal Graphics** option to configure whether to keep IGFX enabled. If user wants to support dual display by internal graphics and external graphics, this Internal Graphics option should be set to Enabled and the above Primary Display option should be set to IGFX.

- | | | | |
|---|-----------------|----------------|----------------|
| → | Auto | | Auto mode |
| → | Disabled | | Disables IGFX. |
| → | Enabled | Default | Enables IGFX. |

→ DVMT Pre-Allocated [32M]

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- | | | |
|---|-----|----------------|
| ▪ | 32M | |
| ▪ | 64M | Default |

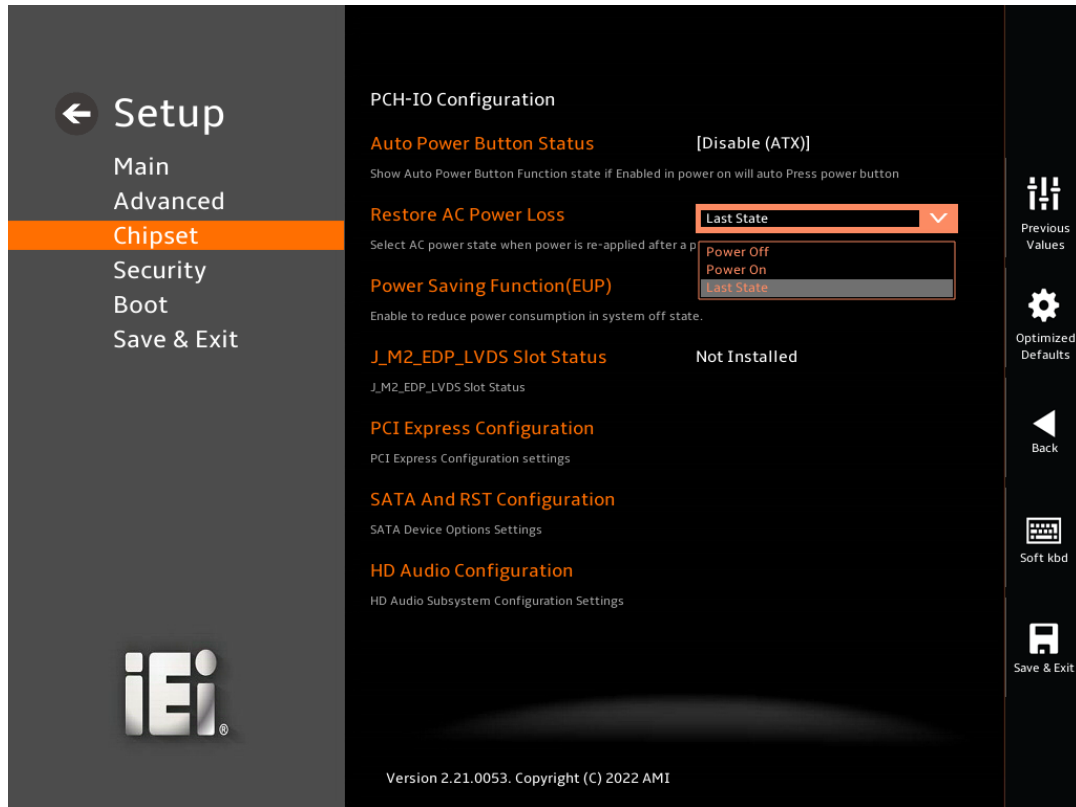
→ DVMT Total Gfx Mem [256M]

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

- | | | |
|---|------|----------------|
| ▪ | 128M | |
| ▪ | 256M | |
| ▪ | MAX | Default |

5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 24**) to configure the PCH parameters.



BIOS Menu 24: PCH-IO Configuration

➔ Auto Power Button Function [Enabled(AT)]

Use the **Auto Power Button Function** BIOS option to show the power mode state. Use the **J_ATX_AT1** to switch the AT/ATX power mode.

- ➔ **Enabled (AT)** The system power mode is AT.
- ➔ **Disabled (ATX)** The system power mode is ATX.

➔ Restore AC Power Loss [Last State]

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system when the power mode is ATX.

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- ➔ **Power Off** The system remains turned off
- ➔ **Power On** The system turns on
- ➔ **Last State** **DEFAULT** The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

➔ **Power Saving Function(EUP) [Disabled]**

Use the **Power Saving Function(EUP)** BIOS option to enable or disable the power saving function.

- ➔ **Disabled** **DEFAULT** Power saving function is disabled.
- ➔ **Enabled** Power saving function is enabled. It will reduce power consumption when the system is off.

➔ **VGA Enable/Disable [Enabled]**

Use the **VGA Enable/Disable** BIOS option to select VGA port Disable or enable

- ➔ **Disabled** VGA function is disabled.
- ➔ **Enabled** **DEFAULT** VGA function is enabled.

➔ **USB Power SW1 [+5V DUAL]**

Use the **USB Power SW1** BIOS option to configure the USB power source for the corresponding USB connectors (Figure 5-3).

- ➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual
- ➔ **+5V** Sets the USB power source to +5V

➔ **USB Power SW2 [+5V DUAL]**

Use the **USB Power SW2** BIOS option to configure the USB power source for the corresponding USB connectors (Figure 5-3).

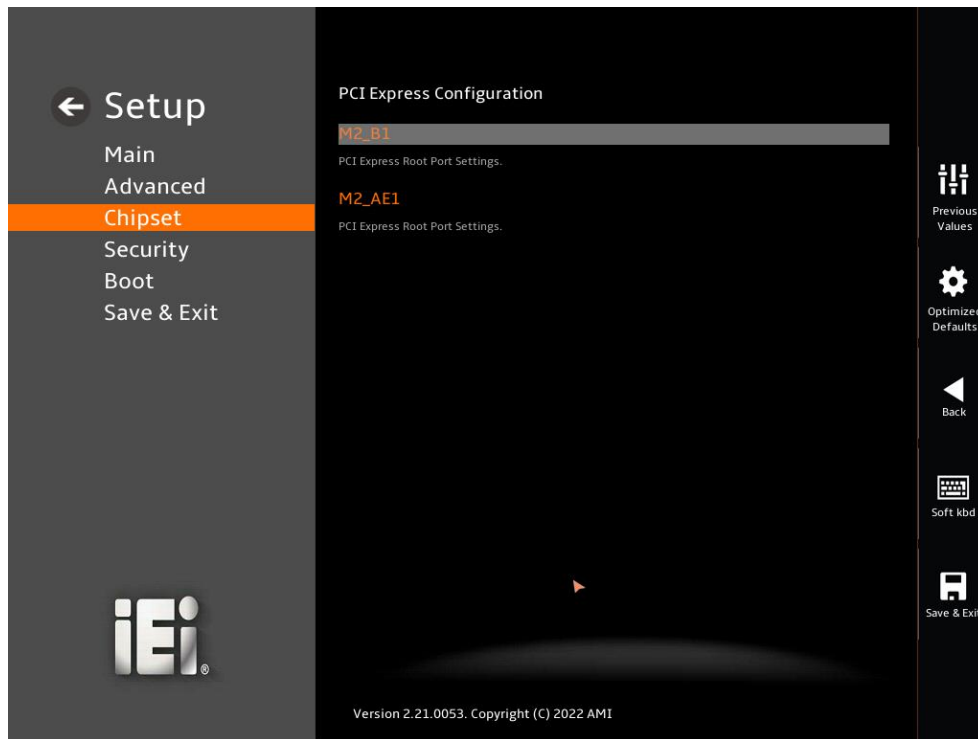
- ➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual
- ➔ **+5V** Sets the USB power source to +5V

| BIOS Options | Configured USB Ports |
|---------------|---|
| USB Power SW1 | K/M_USB1 (external USB 2.0 ports) LAN1_USB1 (external USB 3.2 Gen 2 ports) LAN2_USB2 (external USB 3.2 Gen 1 ports) |
| USB Power SW2 | USB1 (internal USB 2.0 ports) USB2 (internal USB 2.0 ports) USB3-1 (internal USB 3.2 Gen 1 ports) |

Figure 5-3: BIOS Options and Configured USB Ports

5.4.2.1 PCI Express Configuration

Use the **PCI Express Configuration** submenu (**BIOS Menu 25**) to configure the PCI Express slots.

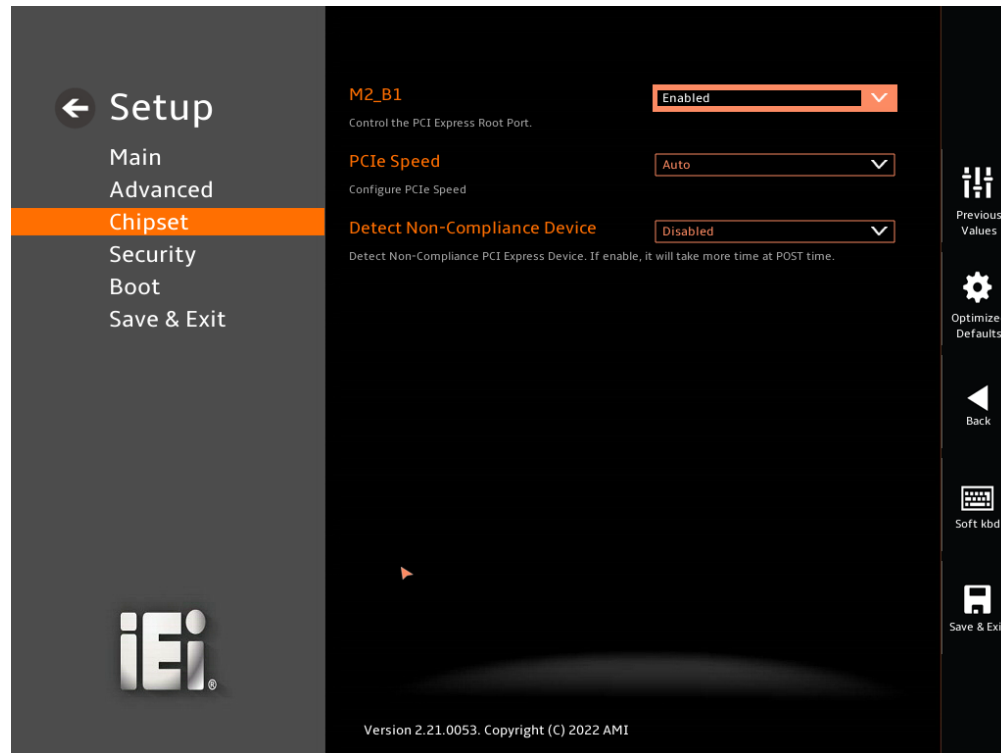


BIOS Menu 25: PCI Express Configuration

5.4.2.1.1 PCIe Root Port Setting

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Use the **PCIEX4_1**, **PCIEX4_2**, **PCIEX16_1**, **M2_A1**, **M2_M1**, **PCIEX4_3** submenu (**BIOS Menu 26**) to configure the PCI Root Port Setting.



BIOS Menu 26: PCIe Slot Configuration Submenu

→ PCIe Speed [Auto]

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

- | | | | |
|---|-------------|----------------|-------------------------------|
| → | Auto | DEFAULT | Auto mode. |
| → | Gen1 | | Configure PCIe Speed to Gen1. |
| → | Gen2 | | Configure PCIe Speed to Gen2. |
| → | Gen3 | | Configure PCIe Speed to Gen3. |

→ Detect Non-Compliance Device [Disabled]

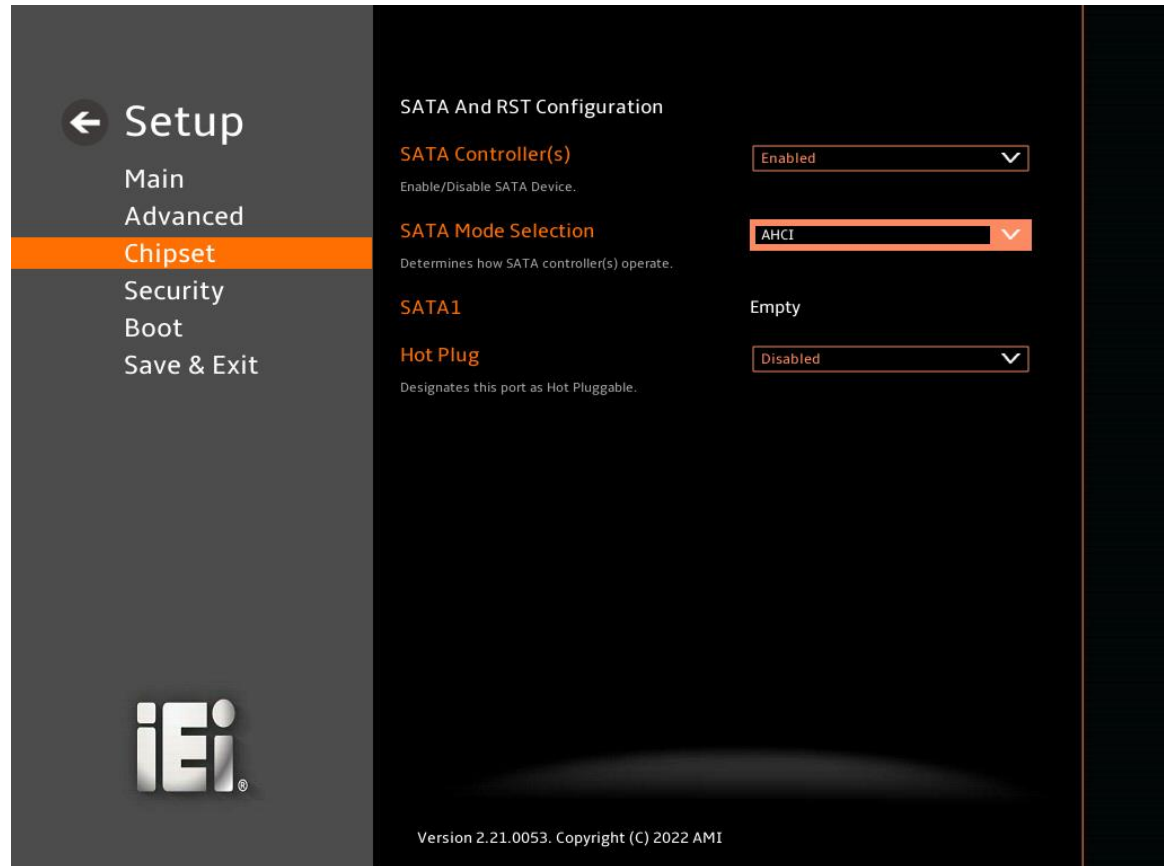
Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

- ➔ **Disabled** **DEFAULT** Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.

- ➔ **Enabled** Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.2 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 27**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 27: SATA Configuration

→ SATA Controller(s) [Enabled]

Use the **SATA Controller(s)** option to configure the SATA controller(s).

- **Enabled** **DEFAULT** Enables the on-board SATA controller(s).
- **Disabled** Disables the on-board SATA controller(s).

→ SATA Mode Selection [AHCI]

Use the **SATA Mode Selection** option to determine how the SATA devices operate.

- **AHCI** **DEFAULT** Configures SATA devices as AHCI device.
- **Intel RST Premium With Intel Optane System Acceleration** Configures SATA devices to the Intel RST Premium With Intel Optane System Acceleration mode.

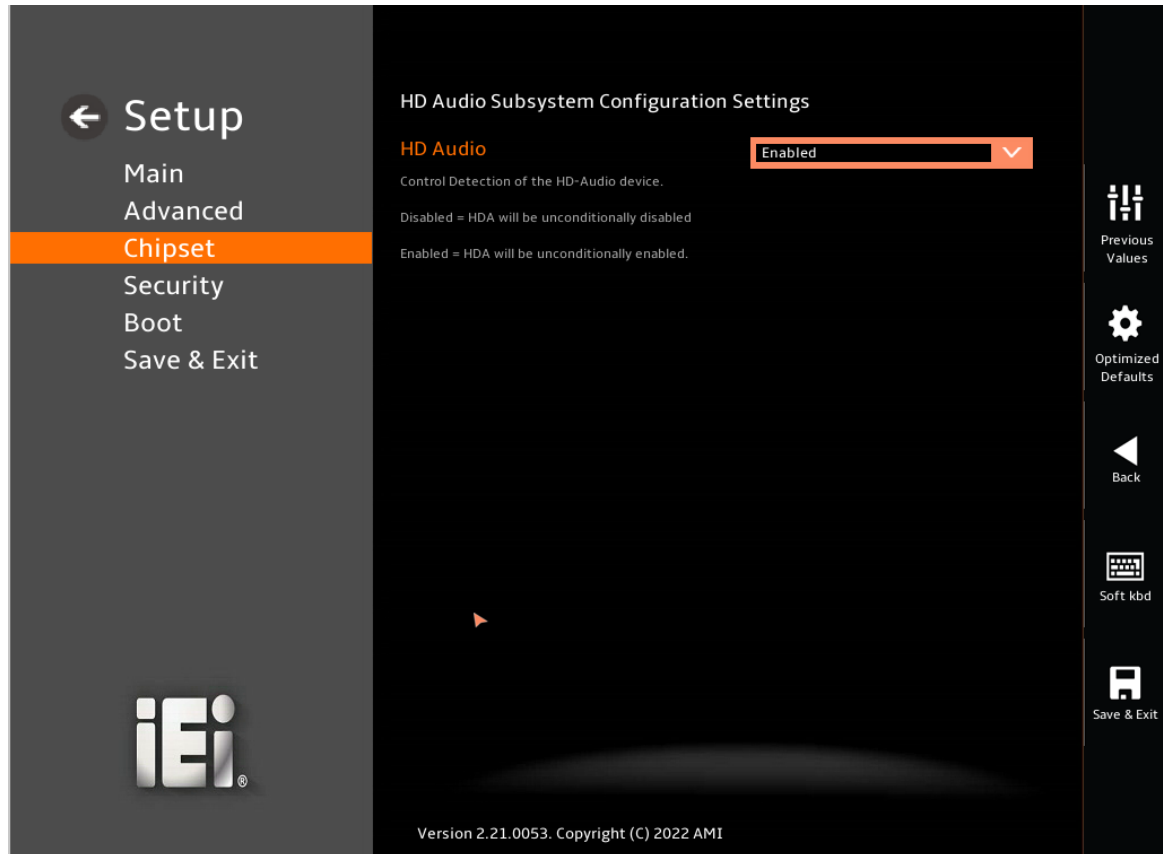
→ **Hot Plug [Disabled]**

Use the **Hot Plug** option (for S_ATA1 to S_ATA4 and M2_M1) to designate the correspondent port as hot-pluggable.

- **Disabled** **DEFAULT** Disables the hot-pluggable function of the SATA port.
- **Enabled** Designates the SATA port as hot-pluggable.

5.4.2.3 HD Audio Configuration

Use the **HD Audio Configuration** menu (**BIOS Menu 28**) to configure the PCH Azalia settings.



BIOS Menu 28: HD Audio Configuration

→ HD Audio [Auto]

Use the **HD Audio** option to enable or disable the High Definition Audio controller.

- **Disabled** The onboard High Definition Audio controller is disabled.
- **Enabled** **DEFAULT** The onboard High Definition Audio controller is enabled.

5.5 Security

Use the **Security** menu (**BIOS Menu 29**) to set system and user passwords.



BIOS Menu 29: Security

➔ Administrator Password

Use the **Administrator Password** to set or change a administrator password.

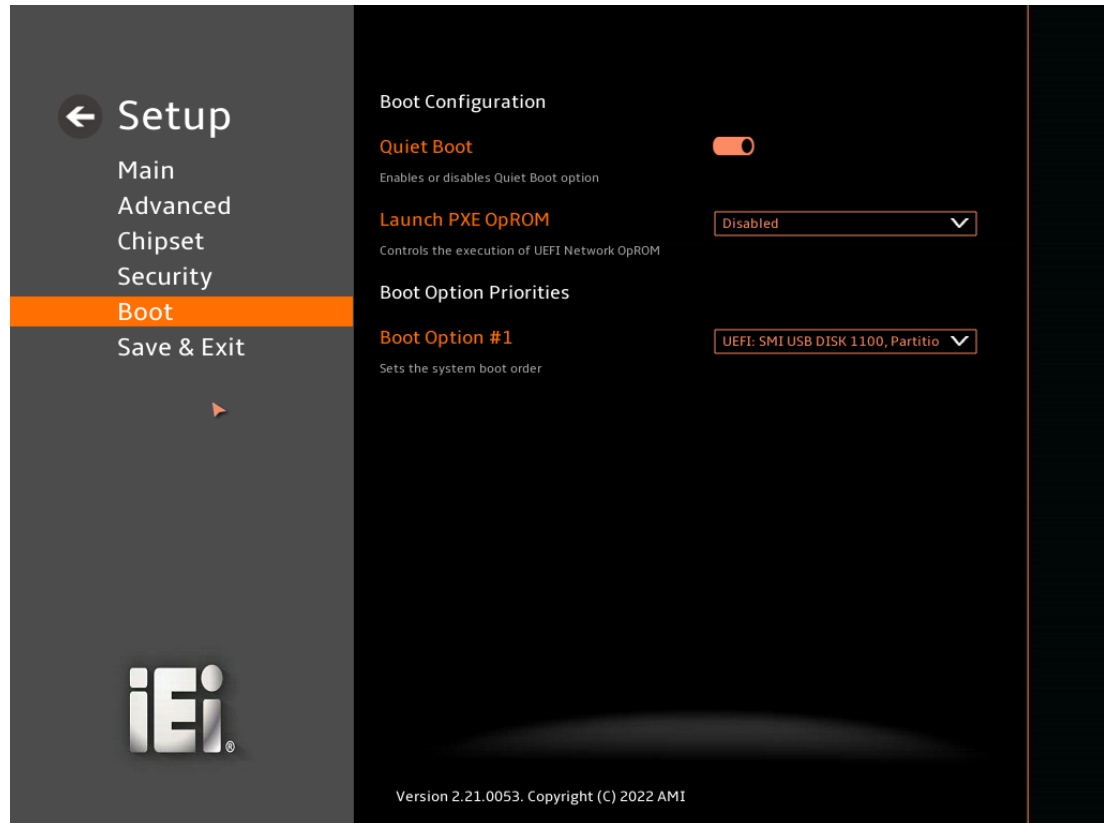
➔ User Password

Use the **User Password** to set or change a user password.

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5.6 Boot

Use the **Boot** menu (**BIOS Menu 30**) to configure system boot options.



BIOS Menu 30: Boot

5.6.1 Boot Configuration

→ Quiet Boot [Enabled]

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

- **Disabled** Normal POST messages displayed
- **Enabled** **DEFAULT** OEM Logo displayed instead of POST messages

→ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

- **Disabled** **DEFAULT** Ignore all PXE Option ROMs
- **Enabled** Load PXE Option ROMs.

→ **Option ROM Messages [Force BIOS]**

Use the **Option ROM Messages** option to set the Option ROM display mode.

- **Force BIOS** **DEFAULT** Sets display mode to force BIOS.
- **Keep Current** Sets display mode to current.

5.6.2 Boot Option Priorities

Use the Boot Option # N to choose the system boots from the peripherals you selected. The following Boot Options are listed as an example.

→ **Boot Option #1**

Sets the system boot order **ADATA SP580** as the first priority.

- **Windows Boot Manager (P1: ADATA SSD SP580 240GB)**
- **Disabled**

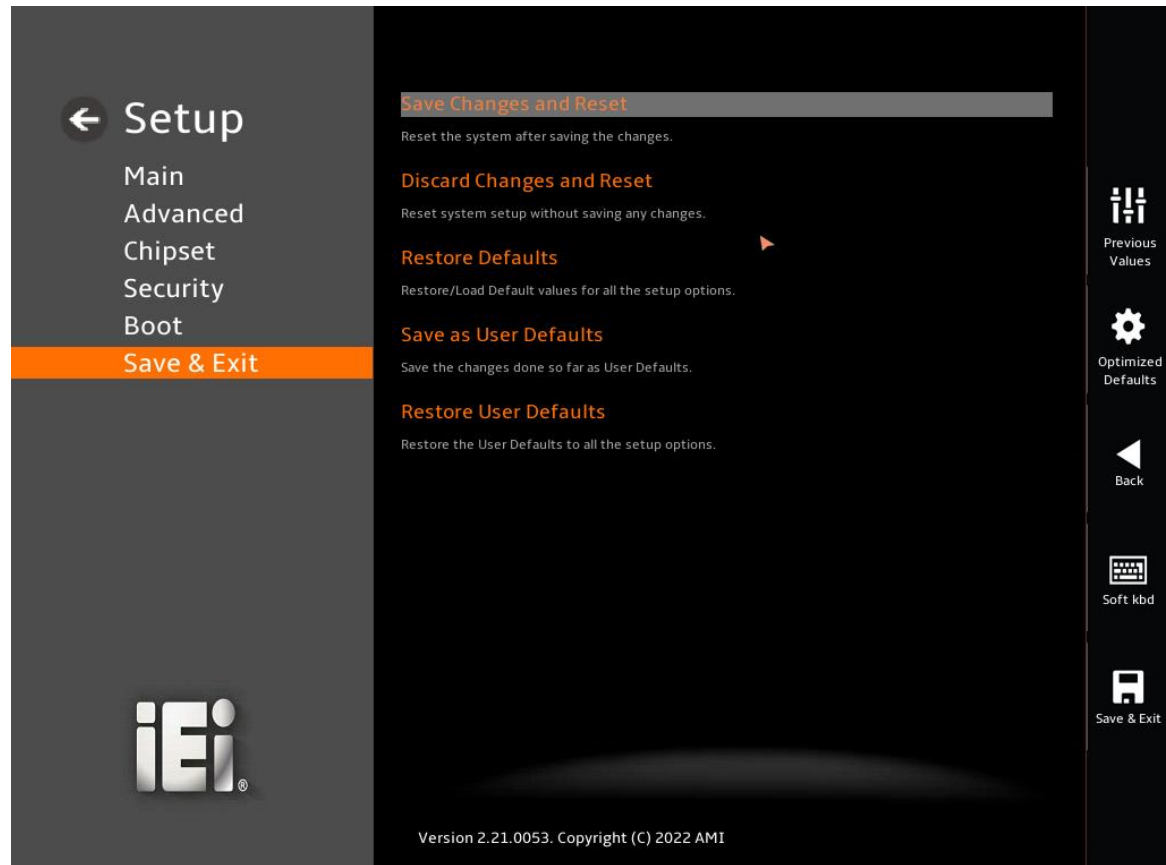
→ **Boot Option #2**

Sets the system boot order **USB Partition 1** as the second priority.

- **UEFI: USB, Partition 1**
- **Disabled**

5.7 Save & Exit

Use the **Safe & Exit** menu (**BIOS Menu 31**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 31: Save & Exit

→ Save Changes and Reset

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

→ Discard Changes and Reset

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

→ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

→ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

→ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY



This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING



This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

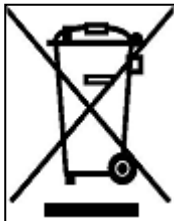
Product Disposal

**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union–If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union–The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Options

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Appendix

D

Watchdog Timer

**NOTE:**

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

| AH – 6FH Sub-function: | |
|-------------------------------|---|
| AL – 2: | Sets the Watchdog Timer's period. |
| BL: | Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup). |

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

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**NOTE:**

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

; INITIAL TIMER PERIOD COUNTER

;

W_LOOP:

;

```

MOV      AX, 6F02H      ;setting the time-out value
MOV      BL, 30         ;time-out value is 48 seconds
INT      15H

```

;

; ADD THE APPLICATION PROGRAM HERE

;

```

CMP      EXIT_AP, 1     ;is the application over?
JNE      W_LOOP        ;No, restart the application

```

```

MOV      AX, 6F02H      ;disable Watchdog Timer
MOV      BL, 0         ;
INT      15H

```

;

; EXIT ;

Appendix

E

Error Beep Code

DRPC-W-TGL

E.1 PEI Beep Codes

| Number of Beeps | Description |
|-----------------|---|
| 1 | Memory not Installed |
| 1 | Memory was installed twice (InstallPeiMemory routine in PEI Core called twice) |
| 2 | Recovery started |
| 3 | DXEIPL was not found |
| 3 | DXE Core Firmware Volume was not found |
| 4 | Recovery failed |
| 4 | S3 Resume failed |
| 7 | Reset PPI is not available |

E.2 DXE Beep Codes

| Number of Beeps | Description |
|-----------------|---|
| 1 | Invalid password |
| 4 | Some of the Architectural Protocols are not available |
| 5 | No Console Output Devices are found |
| 5 | No Console Input Devices are found |
| 6 | Flash update is failed |
| 7 | Reset protocol is not available |
| 8 | Platform PCI resource requirements cannot be met |

**NOTE:**

If you have any question, please contact IEI for further assistance.

Appendix

F

Hazardous Materials Disclosure

DRPC-W-TGL

F.1 RoHS II Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS II Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS II Directive (2015/863/EU).

Please refer to the following table.

| Part Name | Toxic or Hazardous Substances and Elements | | | | | | | | | |
|---|--|--------------|--------------|------------------------------|---------------------------------|--|------------------------------------|------------------------------|-------------------------|-----------------------------|
| | Lead (Pb) | Mercury (Hg) | Cadmium (Cd) | Hexavalent Chromium (CR(VI)) | Polybrominated Biphenyls (PBBs) | Polybrominated Diphenyl Ethers (PBDEs) | Bis(2-ethylhexyl) phthalate (DEHP) | Butyl benzyl phthalate (BBP) | Dibutyl phthalate (DBP) | Diisobutyl phthalate (DIBP) |
| Housing | O | O | O | O | O | O | O | O | O | O |
| Printed Circuit Board | O | O | O | O | O | O | O | O | O | O |
| Metal Fasteners | O | O | O | O | O | O | O | O | O | O |
| Cable Assembly | O | O | O | O | O | O | O | O | O | O |
| Fan Assembly | O | O | O | O | O | O | O | O | O | O |
| Power Supply Assemblies | O | O | O | O | O | O | O | O | O | O |
| Battery | O | O | O | O | O | O | O | O | O | O |
| <p>O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863.</p> <p>X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.</p> | | | | | | | | | | |

F.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有“环境友好使用期限”的标签，此期限是估算这些物质“不会有泄漏或突变”的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

| 部件名称 | 有毒有害物质或元素 | | | | | |
|--------|-----------|--------|--------|--------------|------------|--------------|
| | 铅 (Pb) | 汞 (Hg) | 镉 (Cd) | 六价铬 (CR(VI)) | 多溴联苯 (PBB) | 多溴二苯醚 (PBDE) |
| 壳体 | ○ | ○ | ○ | ○ | ○ | ○ |
| 印刷电路板 | ○ | ○ | ○ | ○ | ○ | ○ |
| 金属螺帽 | ○ | ○ | ○ | ○ | ○ | ○ |
| 电缆组装 | ○ | ○ | ○ | ○ | ○ | ○ |
| 风扇组装 | ○ | ○ | ○ | ○ | ○ | ○ |
| 电力供应组装 | ○ | ○ | ○ | ○ | ○ | ○ |
| 电池 | ○ | ○ | ○ | ○ | ○ | ○ |

○: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。